

DEPARTMENT: ME/AUTOMOBILE

YR/ SEM:II/ III

SUB CODE: EC8396

SUB NAME: ELECTRONICS

& MICROPROCESSORS

UNIT 1-SEMICONDUCTORS & RECTIFIERS

PART A (2 Marks)

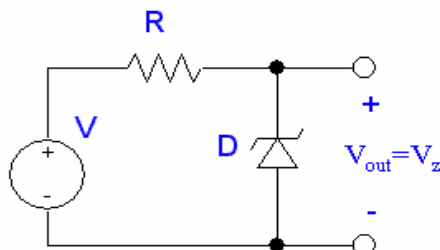
1. Define Rectification. (AUC MAY 2012)

A **rectifier** is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as **rectification**. Rectifiers have many uses, but are often found serving as components of DC power supplies and high-voltage direct current power transmission systems.

2. Define voltage regulation. (AUC MAY 2012)

voltage regulation is a measure of change in the voltage magnitude between the sending and receiving end of a component, such as a transmission or distribution line. Voltage regulation describes the ability of a system to provide near constant voltage over a wide range of load conditions. The term may refer to a passive property that result in more or less voltage drop under various load conditions, or to the active intervention with devices for the specific purpose of adjusting voltage.

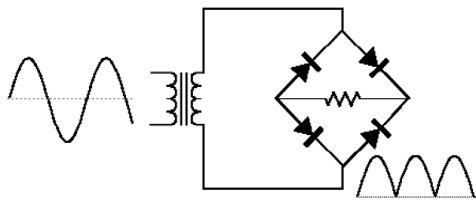
3. Draw the circuit of zener voltage regulator. (AUC MAY 2010)



4. A half wave rectifier having a resistance load of $1\text{K}\Omega$ rectifies an alternating voltage of 325V peak value and the diode has a forward resistance of 100Ω . Calculate its DC power output. (AUC MAY 2010)
5. What is diffusion current? (AUC MAY 2011)

In a non uniformly doped semi conductor charge carriers have a tendency to move from a region of higher concentration to a region of lower concentration. The flow of current due to this process is called diffusion current.

6. Draw the circuit of bridge rectifier with input & output waveforms. (AUC MAY 2011)



7. What is a PN junction. (AUC NOV 2010, NOV 2011)

The junction created when a p type & n type semiconductors joined together is called pn junction. The device formed in such a way is called pn junction diode.

8. Define rectifier. (AUC NOV 2010)

Same as Q1

9. What is a rectifier? What are its types. (AUC NOV 2011)

Same as Q1

The types of rectifiers are,

- Half wave rectifier
- Full wave rectifier
- Bridge rectifier

10. What is meant by dynamic resistance of diode?

Dynamic resistance of a diode can be defined as the ratio of change in voltage across the diode to the change in current through the diode.

$$r = V / I$$

Where

r - Dynamic resistance of a diode

V - change in voltage across the diode

I - change in current through the diode

11. Differentiate between zener breakdown and avalanche breakdown.

Zener breakdown occurs in a reverse biased junction which gives a constant output voltage. Avalanche breakdown does not provide a constant output voltage. This constant voltage from a zener diode can be used as a reference voltage for many regulators.

12. Define Knee voltage of a diode.

Knee voltage of a diode is defined as a breakover voltage above which the forward current increases abruptly. This voltage is also called as breakdown voltage of a diode. It is 0.3 for Ge and 0.7 for Si.

13. What is peak inverse voltage?

The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted by PRV rating). Peak inverse voltage is defined as the maximum reverse voltage that a diode can be subjected to operate in a reverse region so that the diode does not get damaged due to this reverse voltage.

14. What is meant by doping in a semiconductor?

The method of adding impurities to a semiconductor to make them conduct is called doping. It is the process of adding trivalent, pentavalent impurity to the semiconductor which gives rise to P type and N type semiconductor.

15. Give the equation for diode current under reverse bias.

$$I_D = I_0 [e^{VD/nVT} - 1]$$

16. What is diffusion capacitance?

Charge carriers flowing out of a depletion region, which is widened when the junction is reverse biased, there is a large reverse current at first and which slowly decreases to the level of reverse saturation current. The effect is like a discharging of a capacitor called as diffusion capacitance.

17. How do the transition region width and contact potential across a PN junction vary with the applied bias voltage?

The width of the PN junction is widened for a reverse biased junction and narrows for a forward biased junction.

18. What is an ideal diode?

An ideal diode is one which offers zero resistance when forward biased and infinite resistance when reverse biased.

19. Compare ideal diode as a switch.

An ideal diode when forward biased is equivalent to a closed (ON) switch and when reverse biased, it is equivalent to an open (OFF) switch.

20. State the mathematical equation which relates voltage applied across the PN junction diode and current flowing through it.

$$I = I_0 (e^{v/\eta v_T} - 1)$$

21. Define knee/cut-in/threshold voltage of a PN diode.

It is the forward voltage applied across the PN diode below which practically no current flows.

22. What is the effect of junction temperature on cut-in voltage of a PN diode?

Cut-in voltage of a PN diode decreases as junction temperature increases.

23. What is the effect of junction temperature on forward current and reverse current of a PN diode?

For the same forward voltage, the forward current of a PN diode increases and reverse saturation current increases with increase in junction temperature.

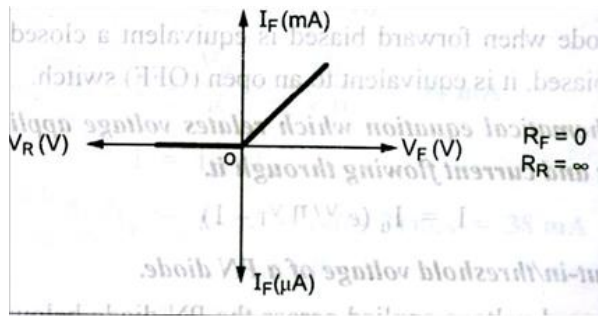
24. Differentiate between breakdown voltage and PIV of a PN diode.

The breakdown voltage of a PN diode is the reverse voltage applied to it at which the PN junction breaks down with sudden rise in reverse current. Whereas, the peak inverse voltage (PIV) is the maximum reverse voltage that can be applied to the PN junction without damage to the junction.

25. Differentiate avalanche and zener breakdowns. Avalanche Breakdown

1. Breakdown occurs due to heavily doped junction and applied strong electric field.
2. Doping level is high.
3. Breakdown occurs at lower voltage compared to avalanche breakdown Zener Breakdown

26. Draw the V-I characteristics of an ideal diode.



26. Differentiate between drift and diffusion currents.

Drift Current

1. It is developed due to potential gradient.
2. This phenomenon is found both in metals and semiconductors

Diffusion Current

1. It is developed due to charge concentration gradient.
2. It is found only in semiconductors.

27. Define transition capacitance of a diode.

Transition Capacitance (\$C_T\$) or Space-charge Capacitance: When a PN-junction is reverse-biased, the depletion region acts like an insulator or as a dielectric.

The P- and N-regions on either side have low resistance and act as the plates. Hence it is similar to a parallel-plate capacitor. This junction capacitance is called transition or space-charge capacitance (\$C_T\$).

It is given by

$$C_T = \frac{\epsilon A}{d}$$

Where, A = Cross-sectional area of depletion region. D = Width (or) thickness of depletion region.

Its typical value is 40 pF.

Since the thickness of depletion layer depends on the amount of reverse bias, C_T can be controlled with the help of applied bias.

This property of variable capacitance is used in varicap or varactor diode. This capacitance is voltage dependent

PART B (8, 16Marks)

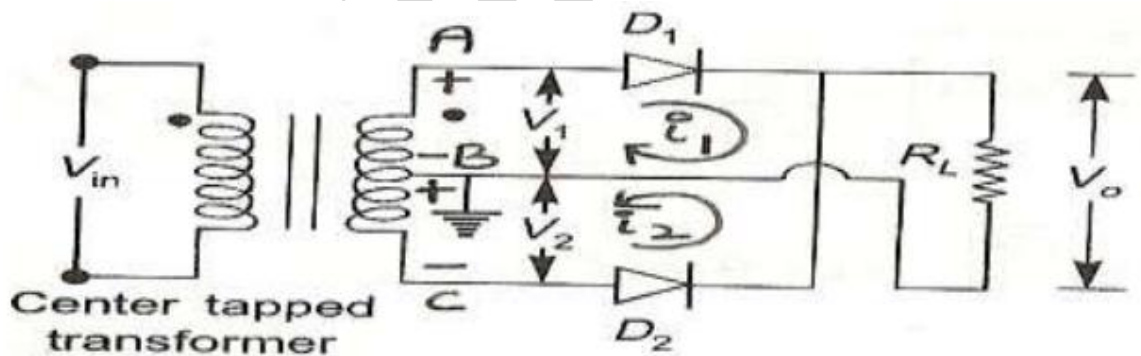
1. Draw & Explain the circuit of full wave rectifier. (AUC MAY 2012, NOV 2011)

Full wave Rectifier using a centre tapped transformer:

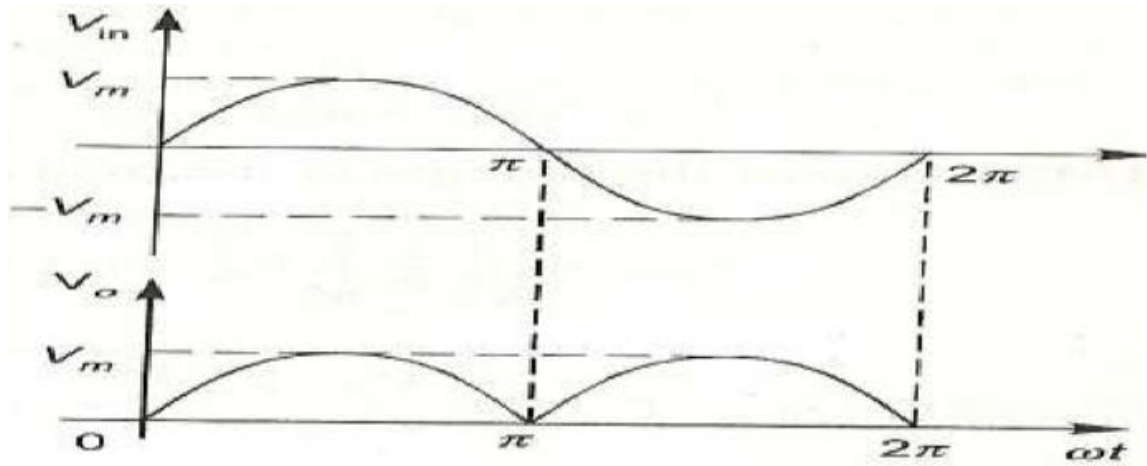
A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer.

A center-tap transformer is the one which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer.

The full wave rectifier is shown in the figure below.



Full-Wave Rectifier.



Voltage Waveforms of a center tapped full wave rectifier

Operation:

During the positive half cycle of the input, the anode of D_1 becomes positive and the anode of D_2 becomes negative. Hence, D_1 conduct and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

Analysis:

Let a sinusoidal voltage V_i be applied to the input of a rectifier. It is given by $V_i = V_m \sin \omega t$

The current i_1 through D_1 and load resistor R_L is given by

$$\begin{aligned} i_1 &= I_m \sin \omega t & \text{for } 0 \leq \omega t \leq \pi \\ i_1 &= 0 & \text{for } \pi \leq \omega t \leq 2\pi \end{aligned}$$

Where $I_m = \frac{V_m}{R_f + R_L}$

Similarly, the current i_2 through diode D_2 and load resistor R_L is given by

$$\begin{aligned} i_2 &= 0 & \text{for } 0 \leq \omega t \leq \pi \\ i_2 &= I_m \sin \omega t & \text{for } \pi \leq \omega t \leq 2\pi \end{aligned}$$

Therefore, the total current flowing through R_L is the sum of the two currents i_1 and i_2 .

i.e., $i_L = i_1 + i_2$.

1. Average Value:

$$\begin{aligned} I_{dc} &= \frac{1}{2\pi} \int_0^{2\pi} i d\theta = \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \theta d\theta \\ &= \frac{I_m}{2\pi} \left[\int_0^{\pi} \sin \theta d\theta - \int_{\pi}^{2\pi} \sin \theta d\theta \right] \\ &= \frac{I_m}{2\pi} [(-2)(-2)] \\ &= \frac{I_m}{2\pi} \cdot 4 = \frac{2I_m}{\pi} = 0.637 I_m. \end{aligned}$$

$I_{dc} = 0.637 I_m.$

$$\therefore I_{DC} \text{ FWR} = 2 I_{DC} \text{ HWR.}$$

2. R.M.S load Current $I_{r.m.s}$

$$I_{rms} = \frac{I_{max}}{\sqrt{2}} = 0.707 I_{max}.$$

3. DC output voltage V_{dc}

$$V_{dc} = I_{dc} \cdot R_L = \frac{2I_m}{\pi} \cdot R_L \quad \text{We know } I_m = \frac{V_m}{R_s + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2V_m R_L}{\pi(R_s + R_f + R_L)}$$

$$\text{If } (R_s + R_f) \ll R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_m$$

$$V_{dc} = 0.637V_m$$

4. Ripple Factor

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483$$

5. Regulation:

The variation of d.c. output voltage as a function of d.c. load current is called *regulation*.

$$\% \text{Regulation} = \frac{V_{\text{no-load}} - V_{\text{full-load}}}{V_{\text{full-load}}} \times 100$$

Voltage regulation =

$$= \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_s)}$$

6. Rectification Efficiency:

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

$$\text{For FWR, } P_{dc} = I_{dc}^2 \cdot R_L = \left(\frac{2}{\pi} \cdot I_m \right)^2 \cdot R_L$$

$$P_{ac} = I_{rms}^2 (R_f + R_s + R_L)$$

$$\left(\frac{I_m}{\sqrt{2}} \right)^2 (R_f + R_s + R_L)$$

$$\eta = \frac{\frac{I_m^2 4}{\pi^2} \cdot R_L}{\frac{I_m^2}{2} \cdot (R_f + R_s + R_L)}$$

$$\text{If } (R_f + R_s) \ll R_L$$

$$\eta = \frac{4}{\pi^2} \cdot \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

7. TRANSFORMER UTILIZATION FACTOR (TUF)

$$\text{a) TUF (Secondary)} = \frac{P_{dc} \text{ delivered to load}}{\text{AC power rating of transformer secondary}}$$

$$\text{b) Since both the windings are used TUF}_{\text{FWR}} = 2 \text{ TUF}_{\text{HWR}} \\ = 2 \times 0.287 = 0.574$$

$$\text{c) TUF primary} = \text{Rated efficiency} = \frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$$

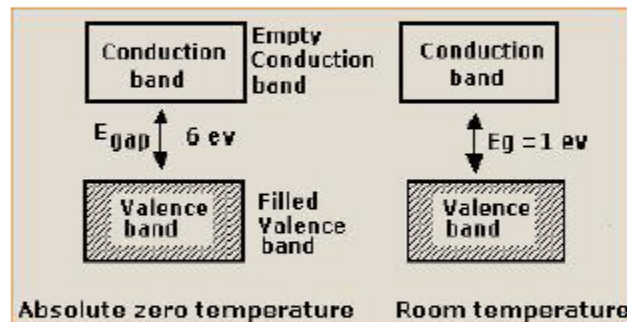
$$\text{d) Average} = \frac{0.812 + 0.574}{2} = 0.693$$

$$8. \text{PIV} = 2 V_m$$

2. Discuss about intrinsic & extrinsic semiconductor. (AUC MAY 2012)

Semiconductors

The valence band is completely filled and conduction band is empty. The E_{gap} is also less i.e., of the order of few eV. At zero kelvin, electrons are not able to cross this forbidden gap and so behave like insulators. But as temperature is increased, electrons in valence band (VB) gain thermal energy and jump to conduction band (CB) and acquire small conductivity at room temperature and so behave like conductors. Hence they are called semiconductors.



Charge carriers in semiconductors

At high temperature, electrons move from valence band to conduction band and as a result a vacancy is created in the valence band at a place where an electron was present before shifting to conduction band. The vacancy is a hole and is seat of positive charge having the same value of electron. Therefore the electrical conduction in semiconductors is due to motion of electrons in conduction band and also due to motion of holes in valence band.

Semiconductor Basics

If Resistors are the most basic passive component in electrical or electronic circuits, then we have to consider the Signal Diode as being the most basic "Active" component. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as it has an exponential I-V relationship and therefore can not be described simply by using Ohm's law as we do for resistors. Diodes are unidirectional semiconductor devices that will only allow current to flow through them in one direction only, acting more like a one way electrical valve, (Forward Biased Condition). But, before we have a look at how signal or power diodes work we first need to understand their basic construction and concept.

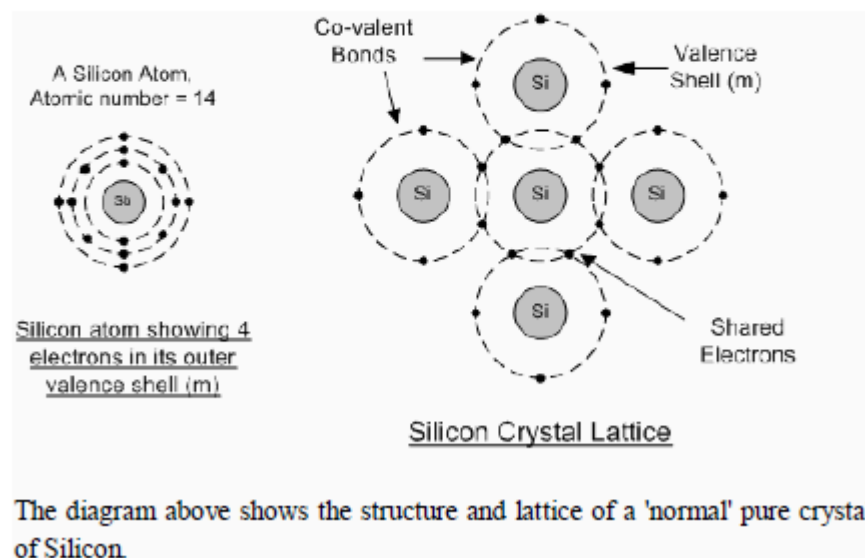
Diodes are made from a single piece of Semiconductor material which has a positive "P-region" at one end and a negative "N-region" at the other, and which has a resistivity value somewhere between that of a conductor and an insulator. But what is a "Semiconductor" material?, firstly let's look at what makes something either a Conductor or an Insulator.

Semiconductor Basics

Semiconductors materials such as silicon (Si), germanium (Ge) and gallium arsenide (GaAs), have electrical properties somewhere in the middle, between those of a "conductor" and an "insulator". They are not good conductors nor good insulators (hence their name "semi"-conductors). They have very few "free electrons" because their atoms are closely grouped together in a crystalline pattern called a "crystal lattice". However, their ability to conduct electricity can be greatly improved by adding certain "impurities" to this crystalline structure thereby, producing more free electrons than holes or vice versa. By controlling the amount of impurities added to the semiconductor material it is possible to control its conductivity. These impurities are called donors or acceptors depending on whether they produce electrons or holes. This process of adding impurity atoms to semiconductor atoms (the order of 1 impurity atom per 10 million (or more) atoms of the semiconductor) is called **Doping**.

The most commonly used semiconductor material by far is **silicon**. It has four valence electrons in its outer most shell which it shares with its adjacent atoms in forming covalent bonds. The structure of the bond between two silicon atoms is such that each atom shares one electron with its neighbour making the bond very stable. As there are very few free electrons available to move from place to place producing an electrical current, crystals of pure silicon (or germanium) are

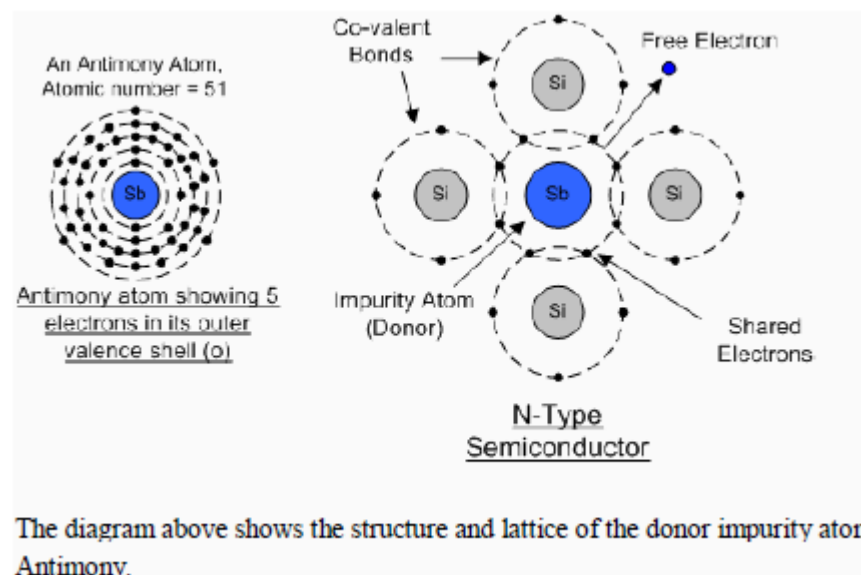
therefore good insulators, or at the very least very high value resistors. Silicon atoms are arranged in a definite symmetrical pattern making them a crystalline solid structure. A crystal of pure silicon (silicon dioxide or glass) is generally said to be an **intrinsic crystal** (it has no impurities).



N-type Semiconductor Basics

In order for our silicon crystal to conduct electricity, we need to introduce an impurity atom such as Arsenic, Antimony or Phosphorus into the crystalline structure making it extrinsic (impurities are added). These atoms have five outer electrons in their outermost co-valent bond to share with other atoms and are commonly called "Pentavalent" impurities. This allows four of the five electrons to bond with its neighbouring silicon atoms leaving one "free electron" to move about when an electrical voltage is applied (electron flow). As each impurity atom "donates" one electron, pentavalent atoms are generally known as "donors".

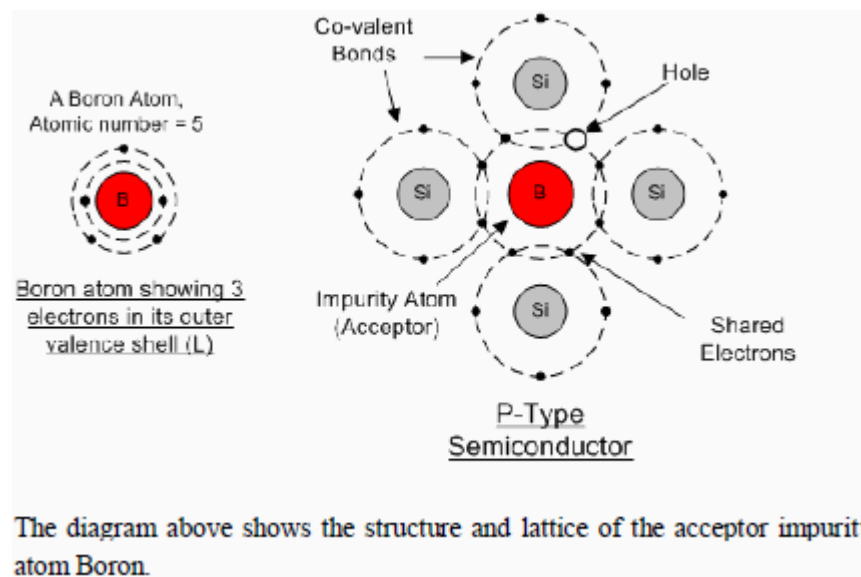
Antimony (symbol Sb) is frequently used as a pentavalent additive as it has 51 electrons arranged in 5 shells around the nucleus. The resulting semiconductor material has an excess of current-carrying electrons, each with a negative charge, and is therefore referred to as "N-type" material with the electrons called "Majority Carriers" and the resultant holes "Minority Carriers". Then a semiconductor material is N-type when its donor density is greater than its acceptor density. Therefore, a N-type semiconductor has more electrons than holes.



P-Type Semiconductor Basics

If we go the other way, and introduce a "Trivalent" (3-electron) impurity into the crystal structure, such as Aluminium, Boron or Indium, only three valence electrons are available in the outermost covalent bond meaning that the fourth bond cannot be formed. Therefore, a complete connection is not possible, giving the semiconductor material an abundance of positively charged carriers known as "holes" in the structure of the crystal. As there is a hole an adjoining free electron is attracted to it and will try to move into the hole to fill it. However, the electron filling the hole leaves another hole behind it as it moves. This in turn attracts another electron which in turn creates another hole behind, and so forth giving the appearance that the holes are moving as a positive charge through the crystal structure (conventional current flow). As each impurity atom generates a hole, trivalent impurities are generally known as "Acceptors" as they are continually "accepting" extra electrons.

Boron (symbol B) is frequently used as a trivalent additive as it has only 5 electrons arranged in 3 shells around the nucleus. Addition of Boron causes conduction to consist mainly of positive charge carriers results in a "P-type" material and the positive holes are called "Majority Carriers" while the free electrons are called "Minority Carriers". Then a semiconductor is P-type when its acceptor density is greater than its donor density. Therefore, a P-type semiconductor has more holes than electrons.



Semiconductor Basics Summary

N-type (e.g. add Antimony)

These are materials which have **Pentavalent** impurity atoms (Donors) added and conduct by "electron" movement and are called, **N-type Semiconductors**.

In these types of materials are:

- 1. The Donors are positively charged.
- 2. There are a large number of free electrons.
- 3. A small number of holes in relation to the number of free electrons.
- 4. Doping gives:
 - positively charged donors.
 - negatively charged free electrons.
- 5. Supply of energy gives:
 - negatively charged free electrons.
 - positively charged holes.

P-type (e.g. add Boron)

These are materials which have **Trivalent** impurity atoms (Acceptors) added and conduct by "hole" movement and are called, **P-type Semiconductors**.

In these types of materials are:

- 1. The Acceptors are negatively charged.
- 2. There are a large number of holes.
- 3. A small number of free electrons in relation to the number of holes.
- 4. Doping gives:
 - negatively charged acceptors.
 - positively charged holes.
- 5. Supply of energy gives:
 - positively charged holes.
 - negatively charged free electrons.

and both P and N-types as a whole, are electrically neutral

In the next tutorial about semiconductors and diodes, we will look at joining the two semiconductor materials, the P-type and the N-type materials to form a **PN Junction** which can be used to produce diodes.

❖ Intrinsic Material

- A perfect semiconductor crystal with no impurities or lattice defects.
- No carriers at 0 K, since the valence band is completely full and the conduction band is completely empty.
- For $T > 0$ K, electrons are thermally excited from the valence band to the conduction band (EHP generation).
- EHP generation takes place due to breaking of covalent bonds \Rightarrow required energy $= E_g$.
- The excited electron becomes free and leaves behind an empty state (hole).
- Since these carriers are created in pairs, the electron concentration (n/cm^3) is always equal to the hole concentration (p/cm^3), and each of these is commonly referred to as the *intrinsic carrier concentration* (n_i).
- Thus, for intrinsic material $n = p$.
- These carriers are not localized in spacings, and are given by quantum mechanical probability distributions.
- Note: $n_i = f(T)$.
- To maintain a steady-state carrier concentration, the carriers must also recombine at the same rate at which they are generated.
- Recombination occurs when an electron from the conduction band makes a transition (direct or indirect) to an empty state in the valence band, thus annihilating the pair.
- At equilibrium, $r_i = g_i$, where g_i and r_i are the generation and recombination rates respectively, and both of these are temperature dependent.
- $g_i(T)$ increases with temperature, and a new carrier concentration n_i is established, such that the higher recombination rate $r_i(T)$ just balances generation.
- At any temperature, the rate of recombination is proportional to the equilibrium concentration of electrons and holes, and can be given by $r_i = \alpha_r n_i p_i = \alpha_r n_i^2 = g_i$ (2.5) where α_r is a constant of proportionality (depends on the mechanism by which recombination takes place).

❖ Extrinsic Material

- In addition to thermally generated carriers, it is possible to create carriers in the semiconductor by purposely introducing impurities into the crystal \Rightarrow *doping*.
- Most common technique for varying the conductivity of semiconductors.
- By doping, the crystal can be made to have predominantly electrons (n-type) or holes (p-type).

- When a crystal is doped such that the equilibrium concentrations of electrons (n_0) and holes (p_0) are different from the intrinsic carrier concentration (n_i), the material is said to be *extrinsic*.
- Doping creates additional levels within the band gap.
- In Si, column V elements of the periodic table (e.g., P, As, Sb) introduce energy levels very near (typically 0.03-0.06 eV) the conduction band.
- At 0 K, these levels are filled with electrons, and very little thermal energy (50 K to 100 K) is required for these electrons to get excited to the conduction band.
- Since these levels donate electrons to the conduction band, they are referred to as the *donor levels*.
- Thus, Si doped with donor impurities can have a significant number of electrons in the conduction band even when the temperature is not sufficiently high enough for the intrinsic carriers to dominate, i.e., $n_0 \gg n_i$, $p_0 \approx 0$ => n-type material, with electrons as *majority carriers* and holes as *minority carriers*.
- In Si, column III elements of the periodic table (e.g., B, Al, Ga, In) introduce energy levels very near (typically 0.03-0.06 eV) the valence band.
- At 0 K, these levels are empty, and very little thermal energy (50 K to 100 K) is required for electrons in the valence band to get excited to these levels, and leave behind holes in the valence band.
- Since these levels accept electrons from the valence band, they are referred to as the *acceptor levels*.
- Thus, Si doped with acceptor impurities can have a significant number of holes in the valence band even at a very low temperature, i.e., $p_0 \gg n_i$, $n_0 \approx 0$ => p-type material, with holes as majority carriers and electrons as minority carriers.
- The extra electron for column V elements is loosely bound and it can be liberated very easily => ionization; thus, it is free to participate in current conduction.
- Similarly, column III elements create holes in the valence band, and they can also participate in current conduction.
- Rough calculation of the ionization energy can be made based on the Bohr's model for H_2 atoms, considering the loosely bound electron orbiting around the tightly bound core electrons. Thus,

$$E = \frac{m_e^* q^4}{2 [4\pi\epsilon_0\epsilon_r]^2 [h/(2\pi)]^2} \quad (2.6) \text{ where } \epsilon_r \text{ is the relative permittivity of Si.}$$

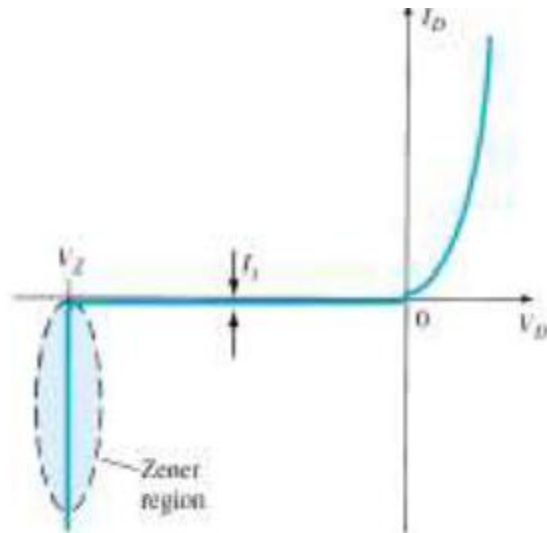
3. What do you mean by zener effect? Explain the characteristics of zener diode. (AUC MAY 2012)

Zener Region:

There is a point where the application of too negative a voltage will result in a sharp change in the characteristics, as shown in the below figure. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *Zener potential* and is given the symbol V_Z . As the voltage across the diode

increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_o will also increase. Eventually, their velocity and associated kinetic energy will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an *ionization* process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined. The avalanche region (V_Z) can be brought closer to the vertical axis by increasing the doping levels in the *p*- and *n*-type materials. However, as V_Z decreases to very low levels, such as -5 V, another mechanism, called *Zener breakdown*, will contribute to the sharp change in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and generate carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of V_Z , this sharp change in the characteristic at any level is called the *Zener region* and diodes employing this unique portion of the characteristic of a *p-n* junction are called *Zener diodes*.

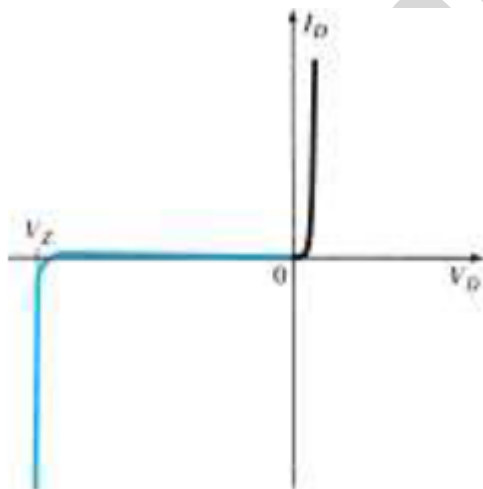
4.
The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted by PRV rating). If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.



Zener breakdown region

ZENER DIODES

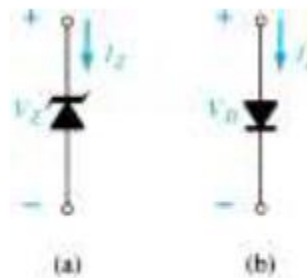
5. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z . The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode.



zener diode characteristics

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in below figure. Both the semiconductor diode and zener diode are presented side by side in the below figure, to ensure that the direction of conduction of each is clearly understood together with the required

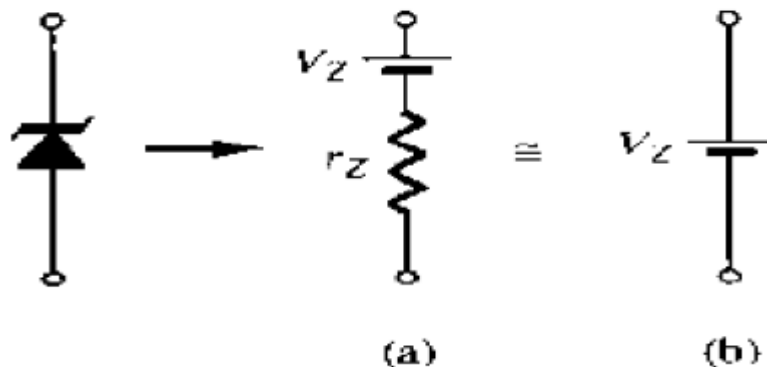
polarity of the applied voltage. For the semiconductor diode the on state will support a current in the direction of the arrow in the symbol. The location of the Zener region can be controlled by varying the doping levels. An increase in doping, producing an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 to 200 V with power ratings from 14 to 50 W. Because of its higher temperature and current capability, silicon is usually preferred in the manufacture of Zener diodes.



Conduction direction:

(a) Zener diode; (b) semiconductor diode

The complete equivalent circuit of the Zener diode in the Zener region includes a small dynamic resistance and dc battery equal to the Zener potential, as shown in below figure



Zener equivalent

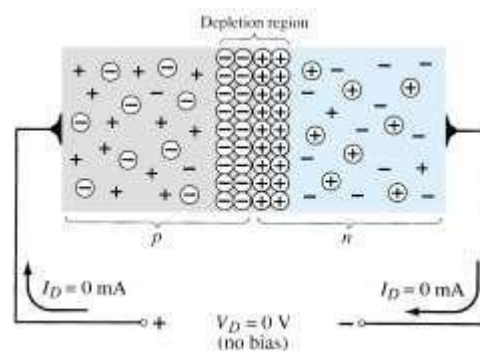
circuit: (a) complete; (b) approximate.

6. Draw & explain the formation of PN junction & explain the working of the diode under forward & reverse bias conditions. (AUC MAY 2010)

PN junction diode

The semiconductor diode is formed by simply bringing these materials together (constructed from the same base—Ge or Si). At the instant the two materials are joined the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region. Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: *no bias* ($V_D = 0$ V), *forward bias* ($V_D > 0$ V), and *reverse bias* ($V_D < 0$ V).

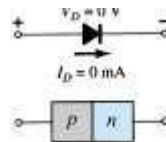
p-n junction with no external bias.



No Applied Bias ($V_D = 0$ V)

7. Under no-bias (no applied voltage) conditions, any minority carriers (holes) in the n -type material that find themselves within the depletion region will pass directly into the p -type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the n -type material. Assume that all the minority carriers of the n -type material that find themselves in the depletion region due to their random motion will pass directly into the p -type material. Similar discussion can be applied to the minority carriers (electrons) of the p -type material. This carrier flow has been indicated in the above figure for the minority carriers of each material. The majority carriers (electrons) of the n -type material must overcome the attractive forces of the layer of positive ions in the n -type material and the shield of negative ions in the p -type material to migrate into the area beyond the depletion region of the p -type material. However, the number of majority carriers is so large in the n -type material that there will invariably be a small number of majority carriers with sufficient kinetic

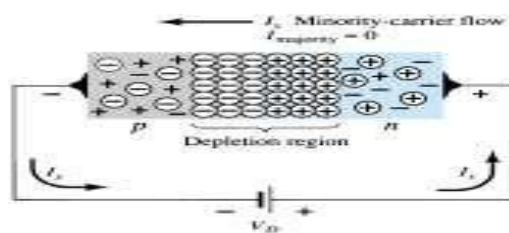
energy to pass through the depletion region into the p -type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the p -type material. The resulting flow due to the majority carriers is also shown in the above figure. In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero. The symbol for a diode is shown in the below figure with the associated n - and p -type regions. Note that the arrow is associated with the p -type component and the bar with the n -type region. As indicated, for $V_D = 0$ V, the current in any direction is 0 mA.



Diode Symbol

Reverse-Bias Condition ($V_D < 0$ V)

8.
If an external potential of V volts is applied across the p - n junction such that the positive terminal is connected to the n -type material and the negative terminal is connected to the p -type material as shown in the below figure. The number of uncovered positive ions in the depletion region of the n -type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the p -type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in the below figure.



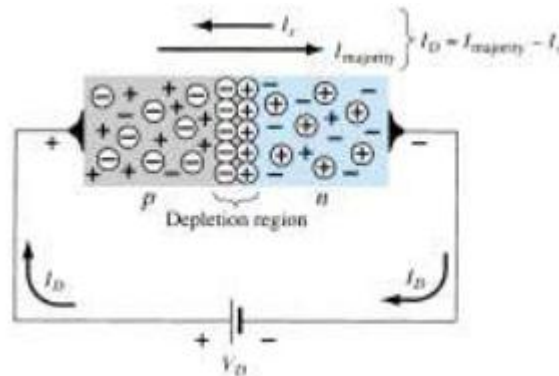
Reverse-biased p - n junction.

The number of minority carriers, however, that find themselves entering the depletion

region will not change, resulting in minority-carrier flow vectors of the same magnitude with no applied voltage the current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_0 .

Forward-Bias Condition ($V_D > 0$ V)

A *forward-bias* condition is established by applying the positive potential to the p -type material and the negative potential to the n -type material as shown in the below figure. A semiconductor diode is forward-biased when the association p -type and positive and n -type and negative has been established.



Forward-biased p - n junction

The application of a forward-bias potential V_D will pressure electrons in the n -type material and holes in the p -type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in the above figure. The resulting minority-carrier flow of electrons from the p -type material to the n -type material (and of holes from the n -type material to the p -type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the n -type material now sees a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p -type material.

Silicon semiconductor diode characteristics.

As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics curve shown before. Note that the vertical scale of characteristic

curve is measured in mill amperes and the horizontal scale in the forward-bias region has a maximum of 1 V. typically, therefore, the voltage across a forward-biased diode will be less than 1 V.

9. Is it possible to replace a zener diode with an ordinary rectifier diode? If no, explain the desired characteristics of zener diode. (AUC MAY 2010)

Same as Q5.

10. Design a Zener voltage regulator for the output voltage of 5V & output current of 200mA. Support your answer with the Zener characteristics & relevant circuit diagram. (AUC MAY 2011)

Same as Q5 for zener characteristics.

11. Explain the operation of open circuited PN junction using energy band structure. (AUC MAY 2011)

Same as Q8

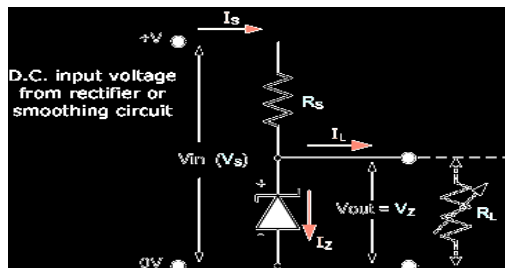
12. What is Zener effect? Explain the Zener diode characteristics and explain how to use it as a voltage regulator. (AUC NOV 2010, NOV 2011)

Same as Q5 for zener effect & characteristics.

The Zener Diode Regulator

Zener Diodes can be used to produce a stabilised voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (R_S), the zener diode will conduct sufficient current to maintain a voltage drop of V_{out} . We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so to does the average output voltage. By connecting a simple zener stabiliser circuit as shown below across the output of the rectifier, a more stable output voltage can be produced.

Zener Diode Regulator



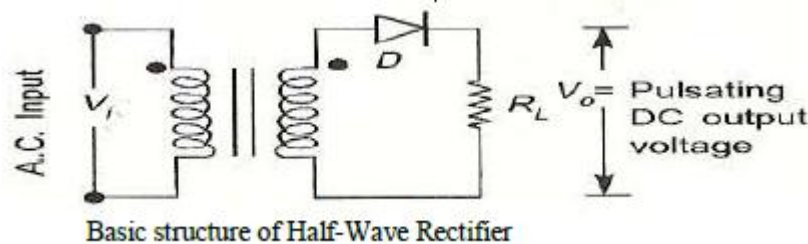
The resistor, R_S is connected in series with the zener diode to limit the current flow through the diode with the voltage source, V_S being connected across the combination. The stabilised output voltage V_{out} is taken from across the zener diode. The zener diode is connected with its cathode terminal connected to the positive rail of the DC supply so it is reverse biased and will be operating in its breakdown condition. Resistor R_S is selected so to limit the maximum current flowing in the circuit. With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the zener diode which in turn dissipates its maximum power. Also a small value of the series resistor R_S will result in a greater diode current when the load resistance R_L is connected and large as this will increase the power dissipation requirement of the diode so care must be taken when selecting the appropriate value of series resistance so that the zener's maximum power rating is not exceeded under this no-load or high-impedance condition. The load is connected in parallel with the zener diode, so the voltage across R_L is always the same as the zener voltage, ($V_R = V_Z$). There is a minimum zener current for which the stabilization of the voltage is effective and the zener current must stay above this value operating under load within its breakdown region at all times. The upper limit of current is of course dependant upon the power rating of the device. The supply voltage V_S must be greater than V_Z . One small problem with zener diode stabiliser circuits is that the diode can sometimes generate electrical noise on top of the DC supply as it tries to stabilise the voltage. Normally this is not a problem for most applications but the addition of a large value decoupling capacitor across the zener's output may be required to give additional smoothing. Then to summarise a little. A zener diode is always operated in its reverse biased condition. A voltage

regulator circuit can be designed using a zener diode to maintain a constant DC output voltage across the load in spite of variations in the input voltage or changes in the load current. The zener voltage regulator consists of a current limiting resistor R_S connected in series with the input voltage V_S with the zener diode connected in parallel with the load R_L in this reverse biased condition. The stabilized output voltage is always selected to be the same as the breakdown voltage V_Z of the diode.

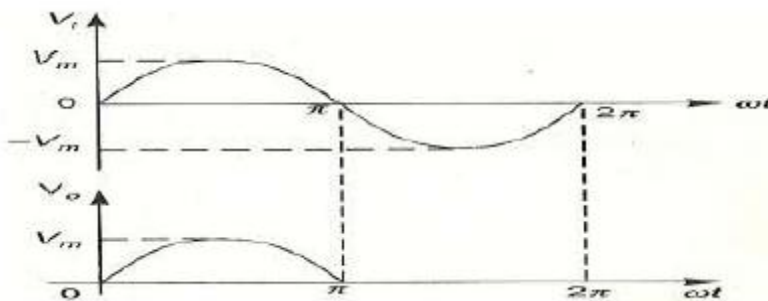
13. Sketch & explain the operation of half & full wave rectifier. (AUC NOV 2010)

Half-Wave Rectifier:

A Half – wave rectifier is one which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.



The half-wave rectifier circuit shown in above figure consists of a resistive load, a rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected in series. The a.c. voltage is applied to the rectifier circuit using step-down transformer.



Input and output waveforms of a Half wave rectifier

The input to the rectifier circuit,

$$V = V_m \sin t$$

Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L . The waveform of the diode current (or) load current is shown in figure.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., $i=0$ and $V_o=0$. Thus for the negative halfcycle no power is delivered to the load.

Where V_m is the maximum value of the secondary voltage.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

- | | |
|------------------------------------|--|
| i) DC output current | ii) DC Output voltage |
| iii) R.M.S. Current | iv) R.M.S. voltage |
| v) Rectifier Efficiency (η) | vi) Ripple factor (γ) |
| vii) Regulation | viii) Transformer Utilization Factor (TUF) |
| ix) Peak Factor (P) | |

Let a sinusoidal voltage V_i be applied to the input of the rectifier.

$$\text{Then } V = V_m \sin \omega t$$

Where V_m is the maximum value of the secondary voltage.

Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and $R_r(=\infty)$ in the reverse direction i.e., in the OFF state.

Now the current 'i' in the diode (or) in the load resistance R_L is given by

$$i = I_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

$$i=0 \quad \text{for } \pi \leq \omega t \leq 2\pi$$

$$\text{where } I_m = \frac{V_m}{R_f + R_L}$$

i) Average (or) DC Output Current (I_{av} or I_{dc}):

The average dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i d(\omega t)$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} 0 \cdot d(\omega t) \right]$$

$$= \frac{1}{2\pi} \left[I_m (-\cos \omega t) \right]_0^{\pi}$$

$$= \frac{1}{2\pi} \left[I_m (+1 - (-1)) \right]$$

$$= \frac{I_m}{\pi} \quad (\text{or}) \quad 0.318 I_m$$

Substituting the value of I_m , we get $I_{dc} = \frac{V_m}{\pi R_f + R_L}$

$$\text{If } R_L \gg R_f \text{ then } I_{dc} = \frac{V_m}{\pi R_L} = 0.318 \frac{V_m}{R_L}$$

ii) Average (or) DC Output Voltage (V_{av} or V_{dc}):

The average dc voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L = \frac{V_m R_L}{\pi R_f + R_L}$$

$$\Rightarrow V_{dc} = \frac{V_m R_L}{\pi R_f + R_L}$$

$$\text{If } R_L \gg R_f \text{ then } V_{dc} = \frac{V_m}{\pi} = 0.318 I_m \quad \therefore V_{dc} = \frac{V_m}{\pi}$$

iii) R.M.S. Output Current (I_{rms}):

The value of the R.M.S. current is given by

$$\begin{aligned} I_{rms} &= \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 d(\omega t) \right]^{\frac{1}{2}} \\ &= \left[\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t d(\omega t) + \frac{1}{2\pi} \int_{\pi}^{2\pi} 0 d(\omega t) \right]^{\frac{1}{2}} \\ &= \left[\frac{I_m^2}{2\pi} \int_0^{\pi} \left(\frac{1 - \cos \omega t}{2} \right) d(\omega t) \right]^{\frac{1}{2}} \\ &= \left[\frac{I_m^2}{4\pi} \left\{ (\omega t) - \frac{1}{2} \sin \omega t \right\} \right]_0^{\pi}^{\frac{1}{2}} \end{aligned}$$

$$\begin{aligned}
 &= \left[\frac{I_m^2}{4\pi} \left\{ \pi - 0 - \frac{\sin 2\pi}{2} + \sin 0 \right\} \right]^{\frac{1}{2}} \\
 &= \left(\frac{I_m^2}{4} \right)^{\frac{1}{2}} \\
 &= \frac{I_m}{2} \\
 \therefore I_{rms} &= \frac{I_m}{2} \quad (\text{or}) \quad I_{rms} = \frac{V_m}{2 R_f + R_L}
 \end{aligned}$$

iv) R.M.S. Output Voltage (V_{rms}):

R.M.S. voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m R_L}{2 R_f + R_L} = \frac{V_m}{2 \left(1 + \frac{R_f}{R_L} \right)}$$

$$\text{If } R_L \gg R_f \text{ then } V_{rms} = \frac{V_m}{2}$$

v) Rectifier efficiency (η):

The rectifier efficiency is defined as the ration of d.c. output power to the a.c. input power i.e.,

$$\therefore \eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = I_{dc}^2 R_L = \frac{I_m^2 R_L}{\pi^2}$$

$$P_{ac} = I_{rms}^2 R_L + R_f = \frac{I_m^2}{4} R_L + R_f$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{I_m^2 R_L}{\pi^2} \times \frac{4}{I_m^2 R_L + R_f} = \frac{4}{\pi^2} \left(\frac{R_L}{R_L + R_f} \right)$$

$$\Rightarrow \eta = \frac{4}{\pi^2} \cdot \frac{1}{\left(1 + \frac{R_f}{R_L}\right)} = \frac{0.406}{1 + \frac{R_f}{R_L}}$$

$$\Rightarrow \% \eta = \frac{40.6}{1 + \frac{R_f}{R_L}}$$

Theoretically the maximum value of rectifier efficiency of a half-wave rectifier is 40.6% when $\frac{R_f}{R_L} = 0$.

vi) Ripple Factor (γ) :

The ripple factor γ is given by

$$\therefore \gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \quad (\text{or}) \quad \therefore \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

$$\Rightarrow \gamma = 1.21$$

vii) Regulation:

The variation of d.c. output voltage as a function of d.c. load current is called *regulation*.

The variation of V_{dc} with I_{dc} for a half-wave rectifier is obtained as follows:

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m / \pi}{R_f + R_L}$$

But $V_{dc} = I_{dc} \times R_L$

$$\begin{aligned} V_{dc} &= \frac{V_m}{\pi} \left[\frac{R_L}{R_f + R_L} \right] \\ &= \frac{V_m}{\pi} \left[1 - \frac{R_f}{R_f + R_L} \right] \end{aligned}$$

$$= \frac{V_m}{\pi} - I_{dc} R_f$$

$$\therefore V_{dc} = \frac{V_m}{\pi} - I_{dc} R_f$$

This result shows that V_{dc} equals $\frac{V_m}{\pi}$ at no load and that the dc voltage decreases linearly with an increase in dc output current. The larger the magnitude of the diode forward resistance, the greater is this decrease for a given current change.

viii) **Transformer Utilization Factor (TUF):**

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$\therefore TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (TUF).

The a.c. power rating of transformer

$$= V_{rms} I_{rms}$$

The secondary voltage is purely sinusoidal hence its rms value is $\frac{1}{\sqrt{2}}$ times maximum

while the current is half sinusoidal hence its rms value is $\frac{1}{2}$ of the maximum

$$\therefore P_{ac(rated)} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{V_m I_m}{2\sqrt{2}}$$

The d.c. power delivered to the load

$$= I_{dc}^2 R_L$$

$$= \left(\frac{I_m}{\pi} \right)^2 R_L$$

$$\therefore TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$= \left(\frac{I_m}{\pi} \right)^2 R_L = \frac{2\sqrt{2}}{V_m I_m}$$

$$= \frac{I_m^2 \cdot R_L \cdot 2\sqrt{2}}{\pi^2 \cdot I_m^2 \cdot R_L} \quad \because V_m \approx I_m R_L$$

$$= 0.287$$

$$\therefore TUF = 0.287$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.

If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver $1000 \times 0.287 = 287$ watts to resistance load.

ix) **Peak Inverse Voltage (PIV):**

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is V_m .

x) **Form factor (F):**

The Form Factor F is defined as

$$F = \text{rms value} / \text{average value}$$

$$F = \frac{I_m / 2}{I_m / \pi}$$

$$F = \frac{0.5 I_m}{0.318 I_m} = 1.57$$

$$F = 1.57$$

xi) **Peak Factor (P):**

The peak factor P is defined as

$$P = \text{Peak Value} / \text{rms value} = \frac{V_m}{V_m / 2} = 2$$

$$P = 2$$

Disadvantages of Half-Wave Rectifier:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Full wave rectifier same as Q1.

14. Explain the VI characteristics of PN diode. (AUC NOV 2011)

Same as Q6

QUESTION BANK

DEPARTMENT: ME

YR/ SEM:II/ III

SUB CODE: ME2255

SUB NAME: ELECTRONICS

& MICROPROCESSORS

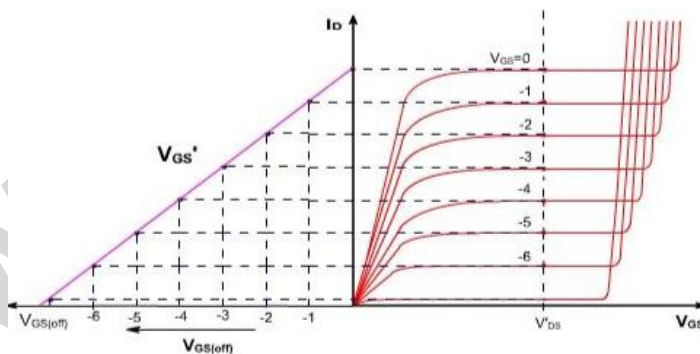
UNIT 2-TRANSISTORS & AMPLIFIERS

PART A (2 Marks)

1. What is the need of transistor biasing? (AUC MAY 2012)

Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components. For bipolar junction transistors the bias point is chosen to keep the transistor operating in the active mode, using a variety of circuit techniques, establishing the Q-point DC voltage and current. A small signal is then applied on top of the Q-point bias voltage, thereby either modulating or switching the current, depending on the purpose of the circuit. The quiescent point of operation is typically near the middle of the DC load line.

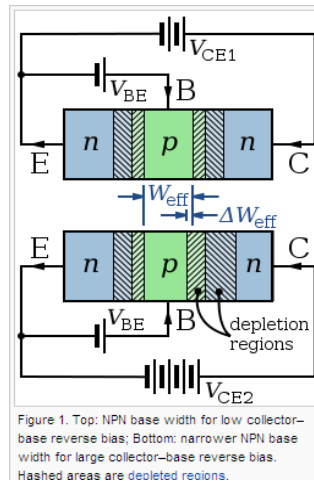
2. Draw the transfer characteristics of FET. (AUC MAY 2012)



3. What is early effect in BJTs? (AUC MAY 2010)

The **Early effect** is the variation in the width of the base in a bipolar junction transistor (BJT) due to a variation in the applied base-to-collector voltage, named after its discoverer James M. Early. A greater reverse bias across the collector–base

junction, for example, increases the collector–base depletion width, decreasing the width of the charge neutral portion of the base.



In Figure 1 the neutral (i.e. active) base is green, and the depleted base regions are hashed light green. The neutral emitter and collector regions are dark blue and the depleted regions hashed light blue. Under increased collector–base reverse bias, the lower panel of Figure 1 shows a widening of the depletion region in the base and the associated narrowing of the neutral base region. The collector depletion region also increases under reverse bias, more than does that of the base, because the collector is less heavily doped. The principle governing these two widths is charge neutrality. The narrowing of the collector does not have a significant effect as the collector is much longer than the base. The emitter–base junction is unchanged because the emitter–base voltage is the same..

Base-narrowing has two consequences that affect the current:

- There is a lesser chance for recombination within the "smaller" base region.
- The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the emitter junction increases.

Both these factors increase the collector or "output" current of the transistor with an increase in the collector voltage. This increased current is shown in Figure 2. Tangents to the characteristics at large voltages extrapolate backward to intercept the voltage axis at a voltage called the **Early voltage**, often denoted by the symbol V_A .

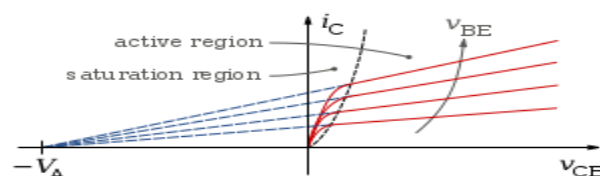


Figure 2. The Early voltage (V_A) as seen in the output-characteristic plot of a BJT

4. Define voltage safety factor of a thyristor. (AUC MAY 2010)

The maximum reverse voltage (cathode positive with respect to anode) that can be applied to an SCR without conduction in the reverse direction, is called the peak reverse voltage (PRV) or peak inverse voltage (PIV).

To avoid puncture of SCR due to uncertain conditions, normal operating voltage is kept well below PRV value of the device. The operating voltage and PRV are related by voltage safety factor V_f defined as $V_f = \text{PRV} / \sqrt{2}x$ (x =rms value of input voltage). The normal value of V_f lies between 2 and 2.5.

5. Define stability factor for BJTs. (AUC MAY 2011)

The process of making operating point independent of temperature changes or variations in transistor parameters is known as stabilization. The rate of change of collector current I_C w.r.t., the collector leakage current I_{CO} at constant β & I_B is called stability factor, S

$$S = dI_C / dI_{CO} \text{ at constant } I_B \text{ \& } \beta$$

6. Write the equation governing intrinsic standoff ratio. (AUC MAY 2011)

The ratio of V_1 to V_{BB} in UJT is called intrinsic standoff ratio & is represented by η

$$\eta = R_{B1} / (R_{B1} + R_{B2})$$

The value of η lies between 0.51 to 0.82

7. What are various types of transistor biasing circuits? (AUC NOV 2012)

- Base resistor method
- Emitter bias method
- Biasing with collector feedback resistor
- Voltage divider bias

8. Mention any two applications of UJT. (AUC NOV 2010)

UJTs are extensively used in oscillators, pulse and voltage sensing circuits

- UJT relaxation oscillator
- Overvoltage detector

9. Compare BJT & FET. (AUC NOV 2011)

S.No	BJT	FET
1	Current controlled device since output is determined on input current	Voltage controlled device, since output depends on field effect of applied voltage
2	Bipolar device becoz current conduction is due to minority & majority carriers	Unipolar device becoz current conduction is due to either minority or majority carriers
3	Has three terminals such as base, emitter & collector	Has three terminals such as source, drain & gate
4	Switching speed is lower	Switching speed is comparatively higher than BJT
5	Small gain bandwidth product than transistor	High gain bandwidth product

10. Define avalanche breakdown. (AUC NOV 2011)

Under normal reverse voltage, a very little reverse current flows through a pn junction. However if the reverse voltage attains a high value, the junction may break down with sudden rise in reverse current. Even at room temperature, electron hole pairs are produced in depletion layer. At large reverse voltage, these electrons acquire high enough velocities to dislodge valence electrons from semiconductor atoms. These electrons in turn free the other valence electrons. In this way we get the avalanche of electrons. This effect is called avalanche effect & the junction breakdown is called avalanche breakdown.

11. What are power transistors? List its applications.

Power

transistors are constructed with n-layer, called drift region between p+ layer and n+ layer. The voltage, current and power ratings are higher. Power diodes operate at high speeds

12. Among CE,CB,CC configuration which one is more popular and why?

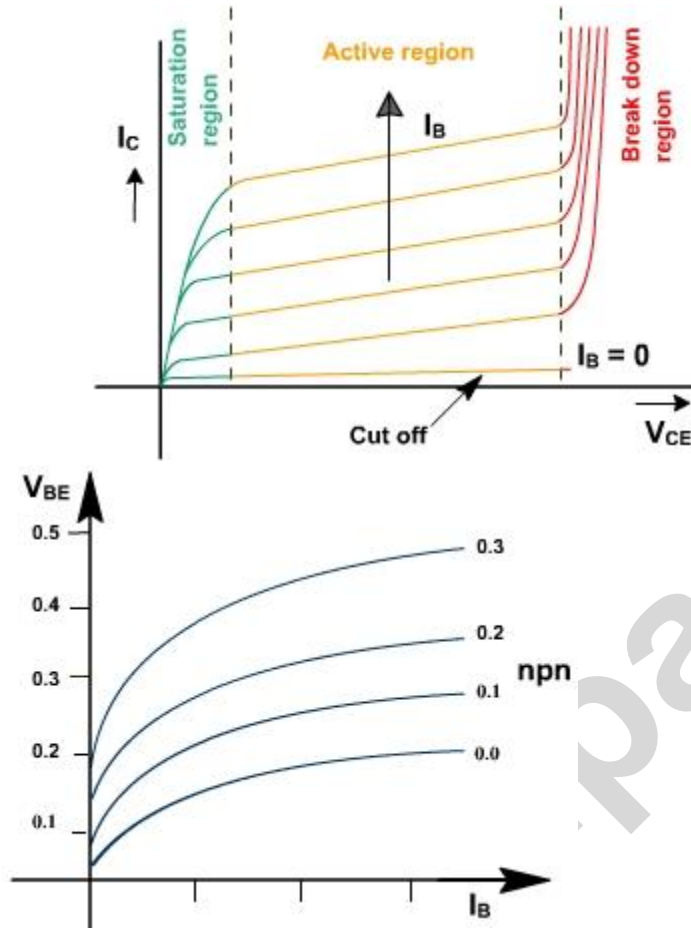
CE configuration is more popular because of its medium input impedance and high voltage gain

13. Calculate β when α is 0.98

$$\beta = \alpha / (\alpha - 1)$$

$$\beta = 0.98 / (1 - 0.98) = 48$$

14. Draw the input and output characteristics of a transistor in CE configuration and mark the cutoff, saturation and active regions.



15. Why is collector region wider than emitter region in BJT?

The collector has to collect the electrons from the emitter region so it is always wider than the emitter region.

16. Name the operating modes of a transistor.

CE, CB, CC configuration

17. What is meant by thermal run away?

As I_{CBO} increases, it increases the collector current which raises the collector base junction temperature. This effect is cumulative. This could produce a significant shift in Q point or in the worst case I_C keeps on increasing until the collector base junction overheats and burns out. This effect is called thermal runaway.

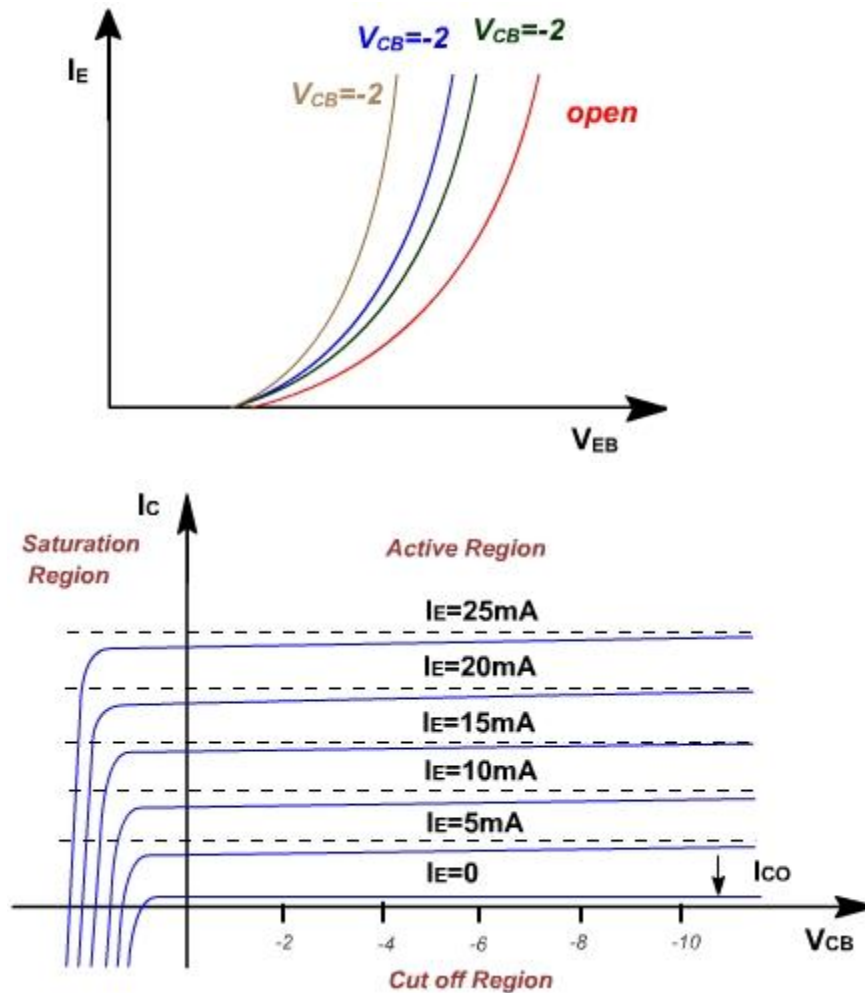
18. Why is it necessary to stabilize the operating point of transistor?

In order to make the transistor in the active region.

19. Derive the relationship between α_{dc} and β_{dc} .

$$\beta = \alpha / (\alpha - 1) \quad \alpha = \beta / (1 + \beta)$$

20. Draw and explain input and output characteristics of a transistor CB configuration



21. List the comparison between CB, CE, CC amplifiers.

Characteristic	Common Base	Common Emitter	Common Collector
Input impedance	Low	Medium	High
Output impedance	Very High	High	Low
Phase Angle	0°	180°	0°
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

22. State the biasing conditions required for the three regions of operation of a BJT.

Emitter base junction – forward biased & Collector base junction reverse biased.

23. What are the types of circuit connections known as configurations, for operating a transistor?

- ☐ Common-Base (CB)
- ☐ Common-Emitter (CE)
- ☐ Common-Collector (CC)

24. What is the relation between α and β of a transistor ?

$$\alpha = \frac{\beta}{\beta + 1}$$

25. What are the regions used when BJT is used as a switch ? Saturation and cut-off regions.

26. What is the thermal resistance of power BJT ?

Thermal resistance is the resistance to the flow of heat. Heat flows from the junction to the surrounding air. Larger the transistor case, smaller the thermal resistance and vice-versa. Thermal resistance is reduced by providing heat sink with the transistor.

27. Why must the base be narrow for the transistor (BJT) action ?

Beta (β) is the ratio of I_C to I_B . I_B becomes less if the base width is narrow. Higher value of β can be obtained with lower value of base current.

23. What is MOSFET? Name its types. (AUC MAY13)

Insulated gate field-effect transistors are unipolar devices just like JFETs: that is, the controlled current does not have to cross a PN junction. There is a PN junction inside the transistor, but its only purpose is to provide that non-conducting depletion region which is used to restrict current through the channel.

Notice how the source and drain leads connect to either end of the N channel, or how the gate lead attaches to a metal plate separated from the channel by a thin insulating barrier. That barrier is sometimes made from silicon dioxide (the primary chemical compound found in sand), which is a very good insulator. Due to this **Metal (gate) - Oxide (barrier) - Semiconductor (channel) construction, the**

IGFET is sometimes referred to as a MOSFET. There are other types of IGFET construction, though, and so "IGFET" is the better descriptor for this general class of transistors. Notice also how there is four connections to the IGFET. In practice, the *substrate* lead is directly connected to the *source* lead to make the two electrically common. Usually, this connection is made internally to the IGFET, eliminating the separate substrate connection, resulting in a three-terminal device with a slightly different schematic symbol.

MOSFET is of two types:

- Depletion type MOSFET
- Enhancement type MOSFET

24. What is pinch off voltage?

Pinch off voltage

The drain current I_D reaches a saturation level called Drain Source Saturation current I_{DSS} at one level of Gate Source voltage V_{GS} called as pinch off voltage, V_p . The channel appears to be pinched off at I_{DSS} . This level of V_{GS} is called pinch of voltage of the channel.

25. Give any two differences between E-MOSFET and D-MOSFET.

S.No	E- MOSFET	D- MOSFET
1	Channel is formed only after the application of reverse voltage to the substrate	During the fabrication process channel is fabricated
2	Enhancement MOSFET cannot be made to operate as Depletion MOSFET	Depletion MOSFET can be made to operate as Enhancement MOSFET by applying a positive gate source voltage
3	Operation does not resemble the operation of JFET	Operation resembles JFET operation

26. Mention the disadvantage of FET compared to BJT.
27. The main disadvantage of FET compared to transistor is it has relatively small gain bandwidth product .
28. Define amplification factor in JFET.
29. Amplification factor μ for a FET is defined as,
- $$\mu = \left(\frac{-\Delta V_{DS}}{\Delta V_{GS}} \right) \Big|_{I_D = (-V_{DS}) / (V_{GS}) \Big|_{I_D = 0}}$$
- $$\mu = r_d * g_m$$
- r_d = Output or drain resistance
- g_m = mutual conductance or transconductance.

PART B (8,16 Marks)

1. Draw & Explain the circuit of a Class B push pull power amplifier & discuss the merits & demerits. (AUC MAY 2012, NOV 2010)

An **electronic amplifier**, **amplifier**, or (informally) **amp** is an electronic device that increases the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude. In this sense, an amplifier modulates the output of the power supply.

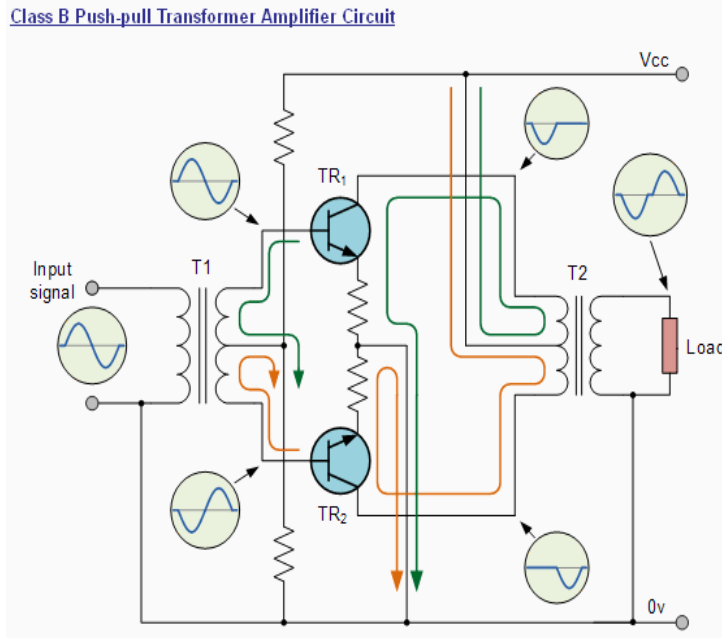
There are four basic types of electronic amplifier: the voltage amplifier, the current amplifier, the transconductance amplifier, and the transresistance amplifier. A further distinction is whether the output is a linear or exponential representation of the input. As well, amplifiers can be categorized by their physical placement in the signal chain.

To improve the full power efficiency of the previous Class A amplifier by reducing the wasted power in the form of heat, it is possible to design the power amplifier circuit with two transistors in its output stage producing what is commonly termed as a **Class B Amplifier** also known as a **push-pull amplifier** configuration.

Push-pull amplifiers use two "complementary" or matching transistors, one being an NPN-type and the other being a PNP-type with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or 180° of the input waveform cycle while the other transistor amplifies the other half or remaining 180°

of the input waveform cycle with the resulting "two-halves" being put back together again at the output terminal.

Then the conduction angle for this type of amplifier circuit is only 180° or 50% of the input signal. This pushing and pulling effect of the alternating half cycles by the transistors gives this type of circuit its amusing "push-pull" name, but are more generally known as the **Class B Amplifier** as shown below.



The circuit above shows a standard **Class B Amplifier** circuit that uses a balanced centre-tapped input transformer, which splits the incoming waveform signal into two equal halves and which are 180° out of phase with each other. Another centre-tapped transformer on the output is used to recombined the two signals providing the increased power to the load. The transistors used for this type of transformer push-pull amplifier circuit are both NPN transistors with their emitter terminals connected together.

Here, the load current is shared between the two power transistor devices as it decreases in one device and increases in the other throughout the signal cycle reducing the output voltage and current to zero. The result is that both halves of the output waveform now swings from zero to twice the quiescent current thereby reducing dissipation. This has the effect of almost doubling the efficiency of the amplifier to around 70%.

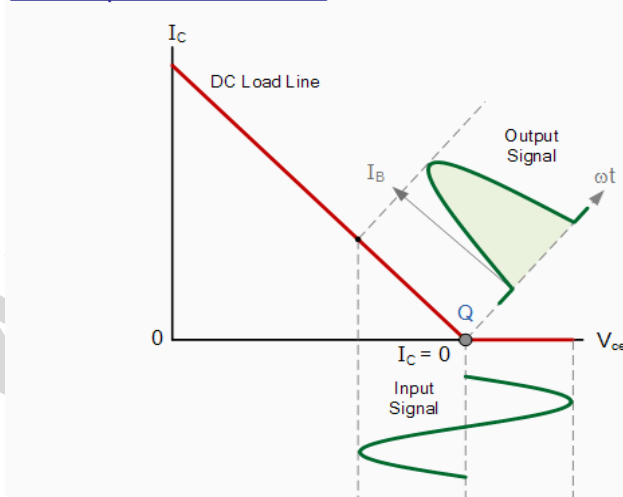
Assuming that no input signal is present, then each transistor carries the normal quiescent collector current, the value of which is determined by the base bias which is at the cut-off point. If the transformer is accurately centre tapped, then the two collector currents will flow in opposite directions (ideal condition) and there will be no magnetization of the transformer core, thus minimizing the possibility of distortion.

When an input signal is present across the secondary of the driver transformer T1, the transistor base inputs are in "anti-phase" to each other as shown, thus if TR1 base goes positive driving the transistor into heavy conduction, its collector current will increase but at the same time the base current of TR2 will go negative further into cut-off and the collector current of this transistor decreases by an equal amount and vice versa. Hence negative halves are amplified by one transistor and positive halves by the other transistor giving this push-pull effect.

Unlike the DC condition, these AC currents are **ADDITIVE** resulting in the two output half-cycles being combined to reform the sine-wave in the output transformers primary winding which then appears across the load.

Class B Amplifier operation has zero DC bias as the transistors are biased at the cut-off, so each transistor only conducts when the input signal is greater than the base-emitter voltage. Therefore, at zero input there is zero output and no power is being consumed. This then means that the actual Q-point of a Class B amplifier is on the V_{ce} part of the load line as shown below.

Class B Output Characteristics Curves



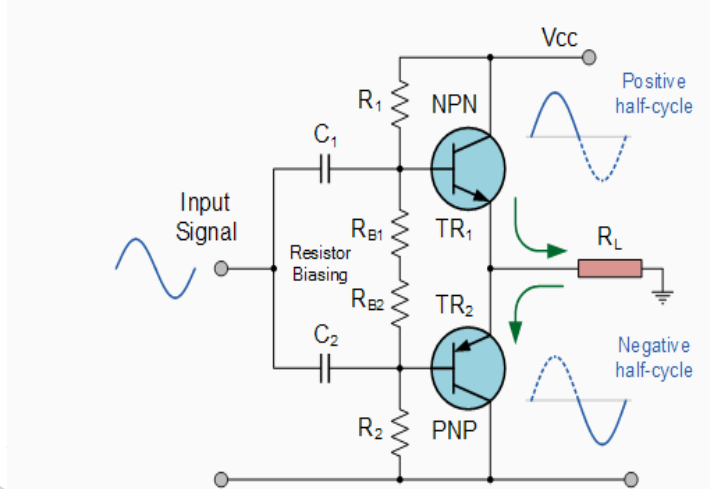
The **Class B Amplifier** has the big advantage over their Class A amplifier cousins in that no current flows through the transistors when they are in their quiescent state (ie, with no input signal), therefore no power is dissipated in the output transistors or

transformer when there is no signal present unlike Class A amplifier stages that require significant base bias thereby dissipating lots of heat - even with no input signal present. So the overall conversion efficiency (η) of the amplifier is greater than that of the equivalent Class A with efficiencies reaching as high as 70% possible resulting in nearly all modern types of push-pull amplifiers operated in this Class B mode.

Transformerless Class B Push-Pull Amplifier

One of the main disadvantages of the Class B amplifier circuit above is that it uses balanced centre-tapped transformers in its design, making it expensive to construct. However, there is another type of Class B amplifier called a **Complementary-Symmetry Class B Amplifier** that does not use transformers in its design therefore, it is transformerless using instead complementary or matching pairs of power transistors. As transformers are not needed this makes the amplifier circuit much smaller for the same amount of output, also there are no stray magnetic effects or transformer distortion to effect the quality of the output signal. An example of a "transformerless" Class B amplifier circuit is given below.

Class B Transformerless Output Stage



Distortion:

Transistors takes approximately 0.7 volts (measured from base to emitter) to get a bipolar transistor to start conducting. In a pure class B amplifier, the output transistors are not "pre-biased" to an "ON" state of operation. This means that the part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as the transition between the two transistors (when they are switching over from one transistor to the other), the transistors do not stop or start

conducting exactly at the zero crossover point even if they are specially matched pairs. The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they are not conducting. The result is that both transistors are turned "OFF" at exactly the same time. A simple way to eliminate crossover distortion in a Class B amplifier is to add two small voltage sources to the circuit to bias both the transistors at a point slightly above their cut-off point. This then would give us what is commonly called an **Class AB Amplifier** circuit. However, it is impractical to add additional voltage sources to the amplifier circuit so pn-junctions are used to provide the additional bias in the form of silicon diodes.

2. What do you mean by negative feedback? List the characteristics & advantages of negative feedback amplifiers. (AUC MAY 2012)

The output signal either voltage or current is sampled and fed back to the input signal using a mixer to form a feedback network. When this feedback signal is out of phase with the input signal, it is called as negative feedback. B is called as feedback ratio.

The gain of the amplifier decreases with the negative feedback. Gain depends on the operating voltages & characteristics of the transistor and also on the feedback network.

Sensitivity is defined as the ratio of percentage change in voltage gain with feedback to percentage change in voltage gain without feedback.

$S = 1/(1 + A\beta)$ A is amplifier gain.

If the feedback network has only stable passive elements, the gain of the amplifier using negative feedback is also stable. This concept of negative feedback is used in amplifiers.

Characteristics of negative feedback:

- Stabilization of gain
- Increase of bandwidth
- Decreased distortion
- Decreased noise
- Increase in input impedance
- Decrease in output impedance

3. Draw the characteristics of FET amplifier & discuss the merits & demerits. (AUC MAY 2012) – same as Q5

4. Draw the circuit diagram & explain the methods of transistor biasing. (AUC MAY 2010)

Fixed Bias or Base Bias:

In order for a transistor to amplify, it has to be properly biased. This means forward biasing the base emitter junction and reverse biasing collector base junction. For linear amplification, the transistor should operate in active region (If I_E increases, I_C increases, V_{CE} decreases proportionally).

The source V_{BB} , through a current limit resistor R_B forward biases the emitter diode and V_{CC} through resistor R_C (load resistance) reverse biases the collector junction as shown in [fig. 1](#).

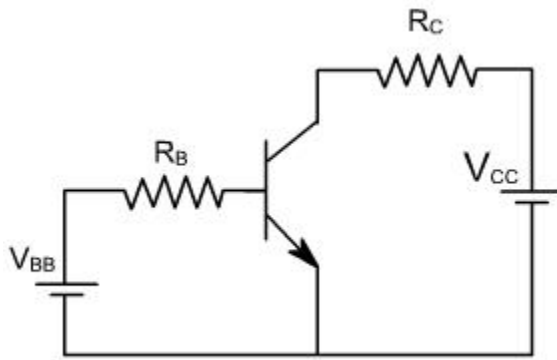


Fig. 1

The dc base current through R_B is given by

$$I_B = (V_{BB} - V_{BE}) / R_B$$

$$\text{or } V_{BE} = V_{BB} - I_B R_B$$

Normally V_{BE} is taken 0.7V or 0.3V. If exact voltage is required, then the input characteristic (I_B vs V_{BE}) of the transistor should be used to solve the above equation. The load line for the input circuit is drawn on input characteristic. The two points of the load line can be obtained as given below

$$\text{For } I_B = 0, \quad V_{BE} = V_{BB}.$$

$$\text{and For } V_{BE} = 0, \quad I_B = V_{BB} / R_B.$$

The intersection of this line with input characteristic gives the operating point Q as shown in [fig. 2](#). If an ac signal is connected to the base of the transistor, then variation in V_{BE} is about Q - point. This gives variation in I_B and hence I_C .

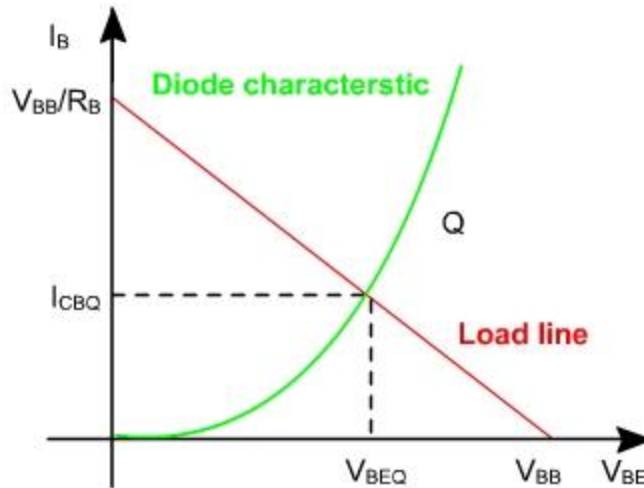


Fig. 2

In the output circuit, the load equation can be written as

$$V_{CE} = V_{CC} - I_C R_C$$

This equation involves two unknown V_{CE} and I_C and therefore can not be solved. To solve this equation output characteristic (I_C vs V_{CE}) is used.

The load equation is the equation of a straight line and given by two points:

$$I_C = 0, \quad V_{CE} = V_{CC}$$

$$\& \quad V_{CE} = 0, \quad I_C = V_{CC} / R_C$$

The intersection of this line which is also called dc load line and the characteristic gives the operating point Q as shown in [fig. 3](#).

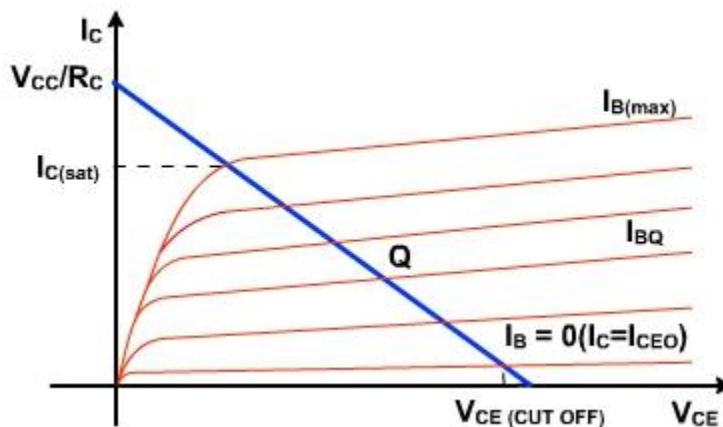


Fig. 3

The point at which the load line intersects with $I_B = 0$ characteristic is known as cut off point. At this point base current is zero and collector current is almost negligibly small. At cut off the emitter diode comes out of forward bias and normal transistor action is lost. To a close approximation,

$$V_{CE} (\text{cut off}) \approx V_{CC} (\text{approximately}).$$

The intersection of the load line and $I_B = I_{B(\text{max})}$ characteristic is known as saturation point. At this point $I_B = I_{B(\text{max})}$, $I_C = I_{C(\text{sat})}$. At this point collector diodes comes out of reverse bias and again transistor action is lost. To a close approximation,

$$I_{C(\text{sat})} \approx V_{CC} / R_C (\text{approximately}).$$

The $I_{B(\text{sat})}$ is the minimum current required to operate the transistor in saturation region. If the I_B is less than $I_{B(\text{sat})}$, the transistor will operate in active region. If $I_B > I_{B(\text{sat})}$ it always operates in saturation region.

If the transistor operates at saturation or cut off points and no where else then it is operating as a switch is shown in [fig. 4](#).

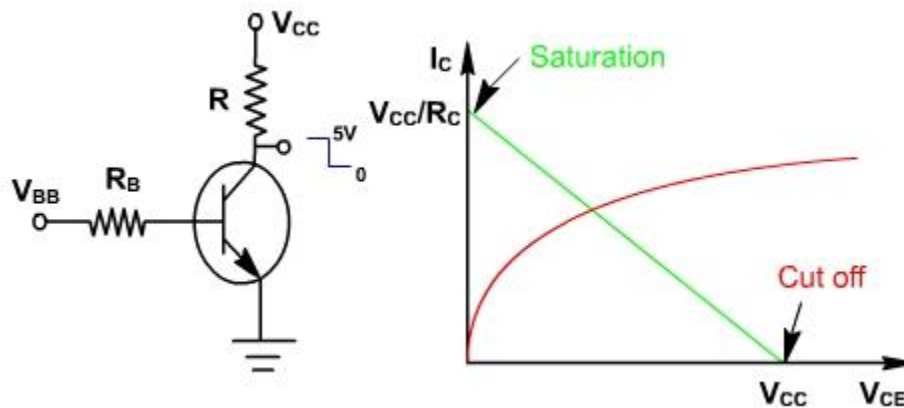


Fig. 4

$$V_{BB} = I_B R_B + V_{BE}$$

$$I_B = (V_{BB} - V_{BE}) / R_B$$

If $I_B > I_{B(\text{sat})}$, then it operates at saturation, If $I_B = 0$, then it operates at cut off.

If a transistor is operating as an amplifier then Q point must be selected carefully. Although we can select the operating point anywhere in the active region by choosing different values of R_B & R_C but the various transistor ratings such as maximum collector dissipation $P_{C(\text{max})}$ maximum collector voltage $V_{C(\text{max})}$ and $I_{C(\text{max})}$ & $V_{BE(\text{max})}$ limit the operating range.

Once the Q point is established an ac input is connected. Due to this the ac source the base current varies. As a result of this collector current and collector voltage also

varies and the amplified output is obtained.

If the Q-point is not selected properly then the output waveform will not be exactly the input waveform. i.e. It may be clipped from one side or both sides or it may be distorted one.

Emitter Feedback Bias:

Fig. 1, shows the emitter feedback bias circuit. In this circuit, the voltage across resistor R_E is used to offset the changes in b_{dc} . If b_{dc} increases, the collector current increases. This increases the emitter voltage which decrease the voltage across base resistor and reduces base current. The reduced base current result in less collector current, which partially offsets the original increase in b_{dc} . The feedback term is used because output current (I_C) produces a change in input current (I_B). R_E is common in input and output circuits.

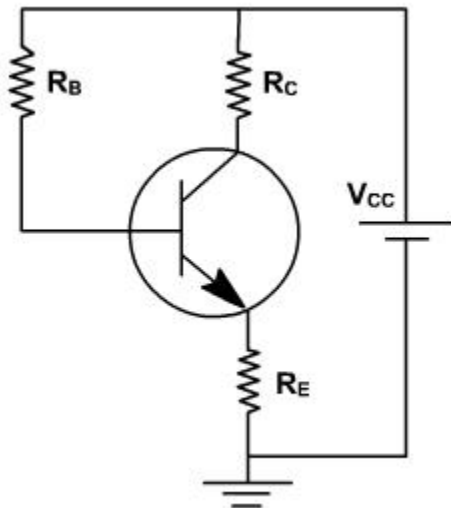


Fig. 1

In this case

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

Since $I_E = I_C + I_B$

$$\therefore \frac{\partial I_B}{\partial I_C} = - \frac{R_E}{R_B + R_E}$$

Therefore,

$$S = \frac{1 + \beta_{dc}}{1 + \beta_{dc} \left(\frac{R_E}{R_B + R_E} \right)} \ll (1 + \beta_{dc})$$

In this case, S is less compared to fixed bias circuit. Thus the stability of the Q point

is better.

Further,

$$I_E \approx I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta_{dc}}}$$

If I_C is to be made insensitive to β_{dc} than

$$R_E \gg \frac{R_B}{\beta_{dc}}$$

R_E cannot be made large enough to swamp out the effects of β_{dc} without saturating the transistor.

Collector Feedback Bias:

In this case, the base resistor is returned back to collector as shown in [fig. 2](#). If temperature increases, β_{dc} increases. This produces more collector current. As I_C increases, collector emitter voltage decreases. It means less voltage across R_B and causes a decrease in base current this decreasing I_C , and compensating the effect of β_{dc} .

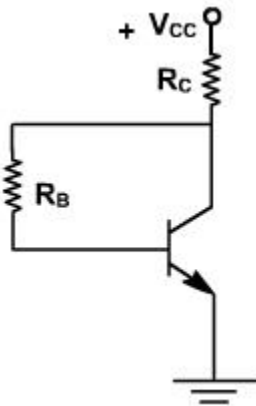


Fig. 2

In this circuit, the voltage equation is given by

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

Circuit is stiff sensitive to changes in β_{dc} . The advantage is only two resistors are used.

Then,

$$\frac{\partial I_B}{\partial I_C} = - \frac{R_C}{R_B + R_C}$$

Therefore,

$$S = \frac{1 + \beta_{dc}}{1 + \frac{R_C \beta_{dc}}{R_B + R_C}} < \frac{1 + \beta_{dc}}{1 + \beta \frac{R_E}{R_B}} < 1 + \beta_{dc}$$

It is better as compared to fixed bias circuit.

Further,

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta_{dc}}}$$

Circuit is still sensitive to changes in β_{dc} . The advantage is only two resistors are used.

Voltage Divider Bias:

If the load resistance R_C is very small, e.g. in a transformer coupled circuit, then there is no improvement in stabilization in the collector to base bias circuit over fixed bias circuit. A circuit which can be used even if there is no dc resistance in series with the collector, is the voltage divider bias or self bias. [fig. 3](#).

The current in the resistance R_E in the emitter lead causes a voltage drop which is in the direction to reverse bias the emitter junction. Since this junction must be forward biased, the base voltage is obtained from the supply through R_1, R_2 network. If $R_b = R_1 \parallel R_2$ equivalent resistance is very – very small, then V_{BE} voltage is independent of I_{CO} and $\frac{\partial I_C}{\partial I_{CO}} \approx 0$. For best stability R_1 & R_2 must be kept small.

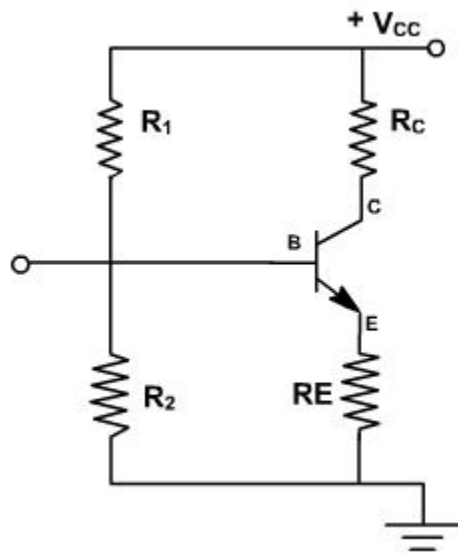


Fig. 3

If I_C tends to increase, because of I_{CO} , then the current in R_C increases, hence base

current is decreased because of more reverse biasing and it reduces I_C .

To analysis this circuit, the base circuit is replaced by its thevenin's equivalent as shown in [fig. 4](#).

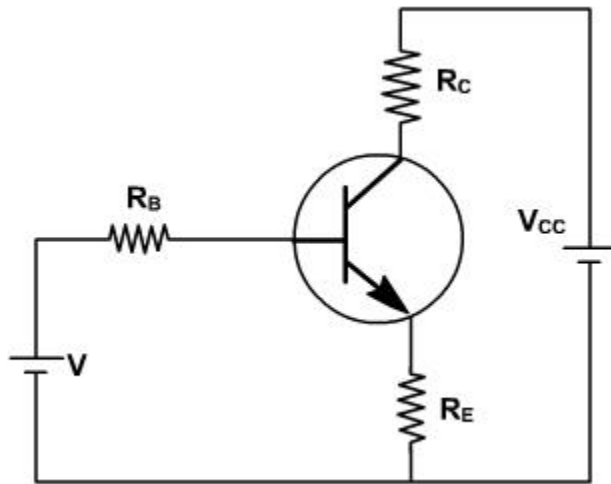


Fig. 4

Thevenin's voltage is

$$V = \frac{R_2}{R_1 + R_2} V_{CC},$$

$$R_b = \frac{R_1 R_2}{R_1 + R_2}$$

R_b is the effective resistance seen back from the base terminal.

$$V = I_B R_b + V_{BE} + (I_B + I_C) R_E$$

If V_{BE} is considered to be independent of I_C , then

$$\frac{\partial I_B}{\partial I_C} = - \frac{R_E}{R_b + R_E}$$

$$S = \frac{1 + \beta_{dc}}{1 + \frac{\beta_{dc} R_E}{R_b + R_E}}$$

$$\text{If } \frac{R_b}{R_c} \rightarrow 0 \text{ then } S \rightarrow 1$$

$$\text{If } \frac{R_b}{R_c} \rightarrow \infty \text{ then } S \rightarrow (1 + \beta_{dc}).$$

The smaller the value of R_b , the better is the stabilization but S cannot be reduced to unity.

Hence I_C always increases more than I_{CO} . If R_b is reduced, then current drawn from the supply increases. Also if R_E is increased then to operate at same Q-point, the magnitude of V_{CC} must be increased. In both the cases the power loss increased and

reduced h .

In order to avoid the loss of ac signal because of the feedback caused by R_E , this resistance is often bypassed by a large capacitance ($> 10 \text{ m F}$) so that its reactance at the frequency under consideration is very small.

Emitter Bias:

Fig. 5, shown the emitter bias circuit. The circuit gets this name because the negative supply V_{EE} is used to forward bias the emitter junction through resistor R_E .

V_{CC} still reverse biases collector junction. This also gives the same stability as voltage divider circuit but it is used only if split supply is available.

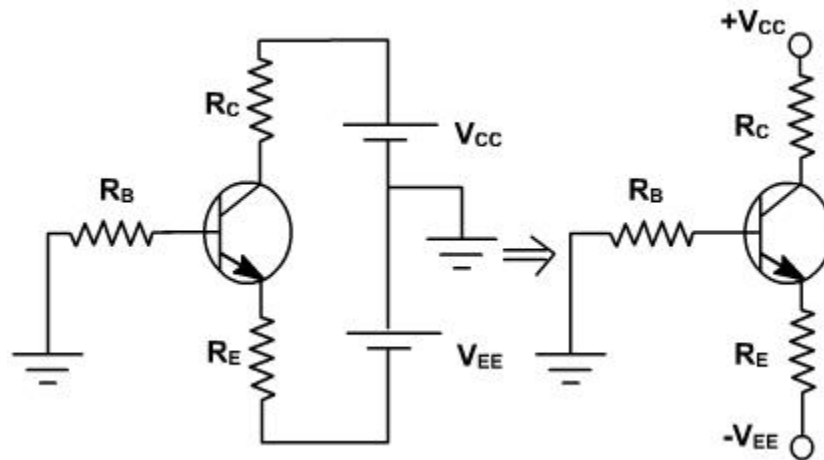


Fig. 5

In this circuit, the voltage equation is given by

$$I_B R_B + V_{BE} + I_E R_E = V_{EE}$$

therefore, $I_B = \frac{I_C}{\beta_{dc}} = \frac{I_E}{\beta_{dc}}$

and $I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta_{dc}}}$

If I_C or I_E is to be independent of β then $R_E \gg \frac{R_B}{\beta_{dc}}$

and then $I_E = \frac{V_{EE} - V_{BE}}{R_E}$

This shows that emitter is virtually at ground potential.

$$V_{CE} = V_{CC} - I_C R_C$$

Normally R_B is selected less than $0.01 \beta_{dc} R_E$

5. Write in detail about the operation of JFET under various biasing conditions. (AUC MAY 2010)

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**.

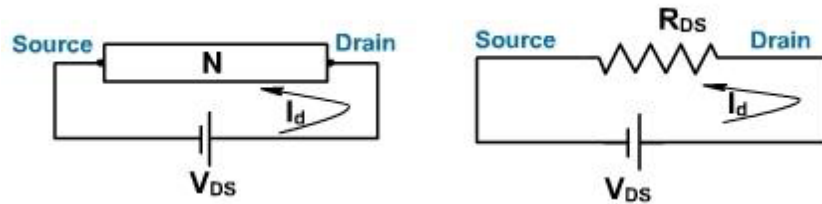
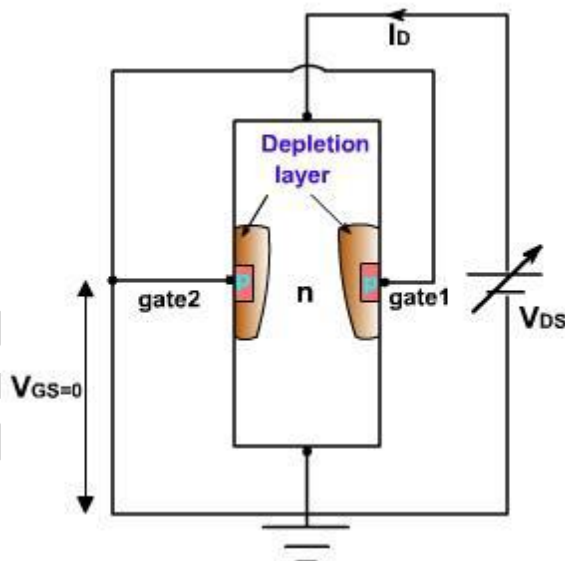


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel. The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leaves the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS} . The resulting current is the drain current I_D . If V_{DS} increases, I_D increases proportionally. Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.



Both the gates are internally connected and they are grounded yielding zero gate source voltage ($V_{GS} = 0$). The word gate is used because the potential applied between gate and source controls the channel width and hence the current. As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers. The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, than points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the non-conducting depletion regions. The width of this channel determines the resistance between drain and source.

Consider now the behavior of drain current I_D vs drain source voltage V_{DS} . The gate source voltage is zero therefore $V_{GS} = 0$. Suppose that V_{DS} is gradually linearly increased from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch off voltage V_P** . At this point further increase in V_{DS} do not produce corresponding increase in I_D . Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS} . (Drain to source current with gate shorted).

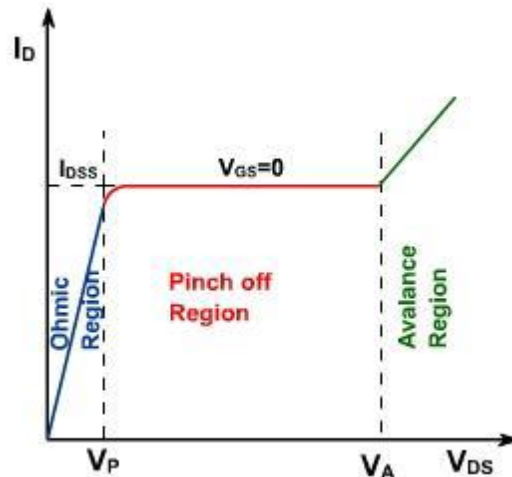
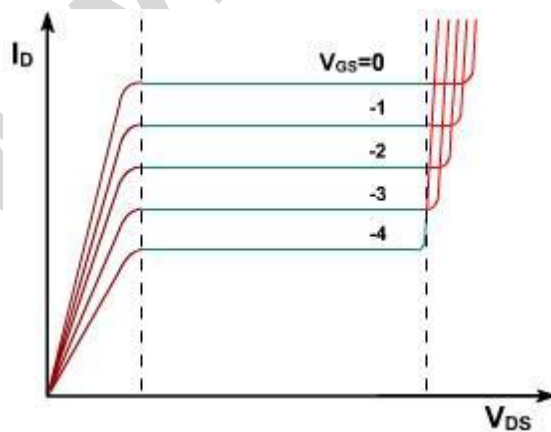
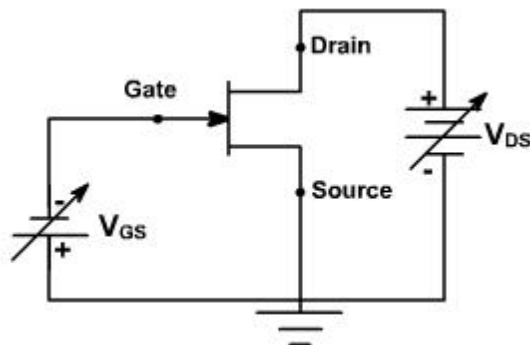


Fig3

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in **fig. 3**.

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig.4**.



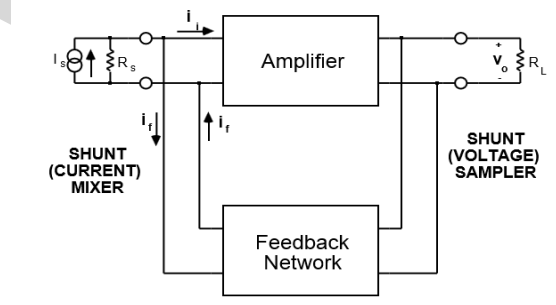
The additional reverse bias, pinch off will occur for smaller values of $|V_{DS}|$, and the maximum drain current will be smaller. A family of curves for different values of V_{GS} (negative) is shown in **fig. 5**.

Suppose that $V_{GS} = 0$ and that due to V_{DS} at a specific point along the channel is +5V with respect to ground. Therefore reverse voltage across either p-n junction is now 5V. If V_{GS} is decreased from 0 to -1V the net reverse bias near the point is $5 - (-1) = 6V$. Thus for any fixed value of V_{DS} , the channel width decreases as V_{GS} is made more negative. Thus I_D value changes correspondingly. When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized $V_{GS(off)}$. It is same as pinch off voltage. Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. $I_D = I_S$. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

6. If the various parameters of CE amplifier which uses the self bias method are $V_{CC}=12V$, $R_1=10K\Omega$, $R_2=5K\Omega$, $R_C=1 K\Omega$, $R_E= 2 K\Omega$ and $\beta=100$ find (i) the co ordinates of operating point (ii) the stability factor assuming the transistor to be silicon. (AUC MAY 2011)
7. Why do we prefix negative feedback system? Explain the operation of voltage shunt feedback with required diagrams. (AUC MAY 2011)

CURRENT-IN, VOLTAGE-OUT

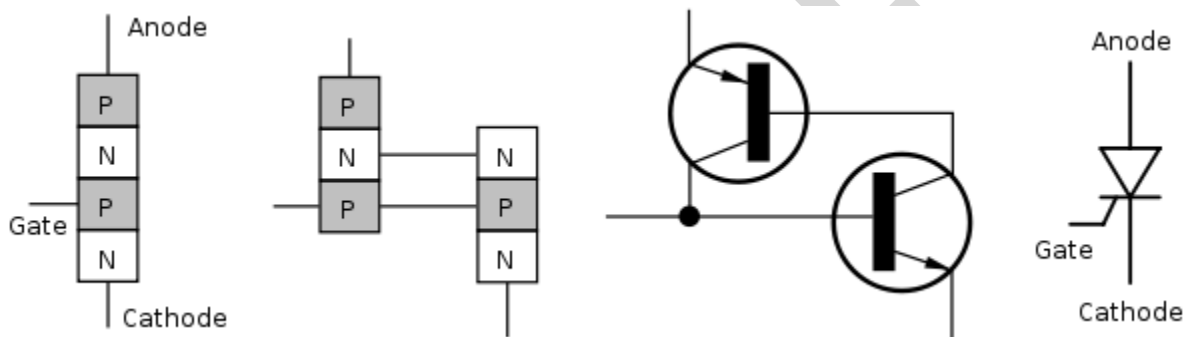
(SHUNT [CURRENT] MIXING, VOLTAGE-SAMPLING)



8. Explain the characteristics of SCR, TRIAC & DIAC. (AUC NOV 2010)

SCR Characteristics:

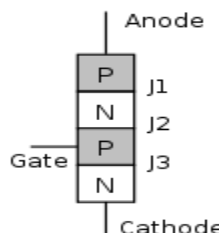
The SCR also called as thyristor is a four-layered, three terminal semiconductor device, with each layer consisting of alternately [N-type](#) or [P-type](#) material, for example P-N-P-N. The main terminals, labelled anode and cathode, are across all four layers. The control terminal, called the gate, is attached to p-type material near the cathode. (A variant called an SCS—Silicon Controlled Switch—brings all four layers out to terminals.) The operation of a thyristor can be understood in terms of a pair of tightly coupled [bipolar junction transistors](#), arranged to cause a self-latching action:



Thyristors have three states:

1. Reverse blocking mode — Voltage is applied in the direction that would be blocked by a diode
2. Forward blocking mode — Voltage is applied in the direction that would cause a diode to conduct, but the thyristor has not been triggered into conduction
3. Forward conducting mode — The thyristor has been triggered into conduction and will remain conducting until the forward current drops below a threshold value known as the "holding current"

The thyristor has three [p-n junctions](#) (serially named J_1 , J_2 , J_3 from the anode).



Layer diagram of thyristor.

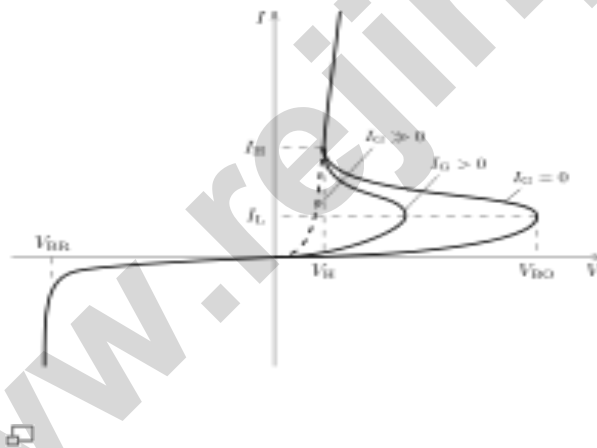
When the anode is at a positive potential V_{AK} with respect to the cathode with no voltage applied at the gate, junctions J_1 and J_3 are forward biased, while junction J_2 is reverse biased. As J_2 is reverse biased, no conduction takes place (Off state). Now if V_{AK} is increased beyond the breakdown voltage V_{BO} of the thyristor, avalanche breakdown of J_2 takes place and the thyristor starts conducting (On state).

If a positive potential V_G is applied at the gate terminal with respect to the cathode, the breakdown of the junction J_2 occurs at a lower value of V_{AK} . By selecting an appropriate value of V_G , the thyristor can be switched into the on state quickly.

Once avalanche breakdown has occurred, the thyristor continues to conduct, irrespective of the gate voltage, until: (a) the potential V_{AK} is removed or (b) the current through the device (anode-cathode) is less than the holding current specified by the manufacturer. Hence V_G can be a voltage pulse, such as the voltage output from a UJT relaxation oscillator.

The gate pulses are characterized in terms of gate trigger voltage (V_{GT}) and gate trigger current (I_{GT}). Gate trigger current varies inversely with gate pulse width in such a way that it is evident that there is a minimum gate charge required to trigger the thyristor.

switching characteristics



V - I characteristics.

In a conventional thyristor, once it has been switched on by the gate terminal, the device remains latched in the on-state (*i.e.* does not need a continuous supply of gate current to remain in the on state), providing the anode current has exceeded the latching current (I_L). As long as the anode remains positively biased, it cannot be switched off until the anode current falls below the holding current (I_H).

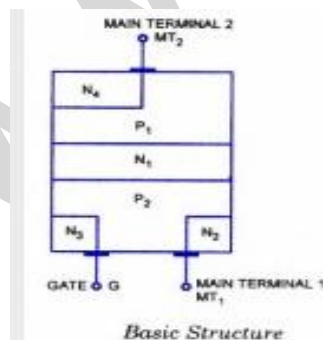
A thyristor can be switched off if the external circuit causes the anode to become negatively biased (a method known as natural, or line, commutation). In some applications this is done by switching a second thyristor to discharge a capacitor into the cathode of the first thyristor. This method is called forced commutation.

After the current in a thyristor has extinguished, a finite time delay must elapse before the anode can again be positively biased *and* retain the thyristor in the off-state. This minimum delay is called the circuit commutated turn off time (t_Q). Attempting to positively bias the anode within this time causes the thyristor to be self-triggered by the remaining charge carriers (holes and electrons) that have not yet recombined.

For applications with frequencies higher than the domestic AC mains supply (e.g. 50 Hz or 60 Hz), thyristors with lower values of t_Q are required. Such fast thyristors can be made by diffusing heavy metal ions such as gold or platinum which act as charge combination centers into the silicon. Today, fast thyristors are more usually made by electron or proton irradiation of the silicon, or by ion implantation. Irradiation is more versatile than heavy metal doping because it permits the dosage to be adjusted in fine steps, even at quite a late stage in the processing of the silicon.

TRIAC Characteristics

TRIAC, from **Triode for Alternating Current**, is a genericized tradename for an electronic component that can conduct current in either direction when it is triggered (turned on), and is formally called a **bidirectional triode thyristor** or **bilateral triode thyristor**.



TRIACs are part of the thyristor family and are closely related to silicon-controlled rectifiers (SCR). However, unlike SCRs, which are unidirectional devices (that is. can

conduct current only in one direction), TRIACs are bidirectional and so current can flow in either direction. Another difference from SCRs is that TRIAC current flow can be enabled by either a positive or negative current applied to its *gate* electrode, whereas SCRs can be triggered only by current going into the gate. To create a triggering current, a positive or negative voltage has to be applied to the gate with respect to the MT1 terminal (otherwise known as A1).

Once triggered, the device continues to conduct until the current drops below a certain threshold called the holding current.

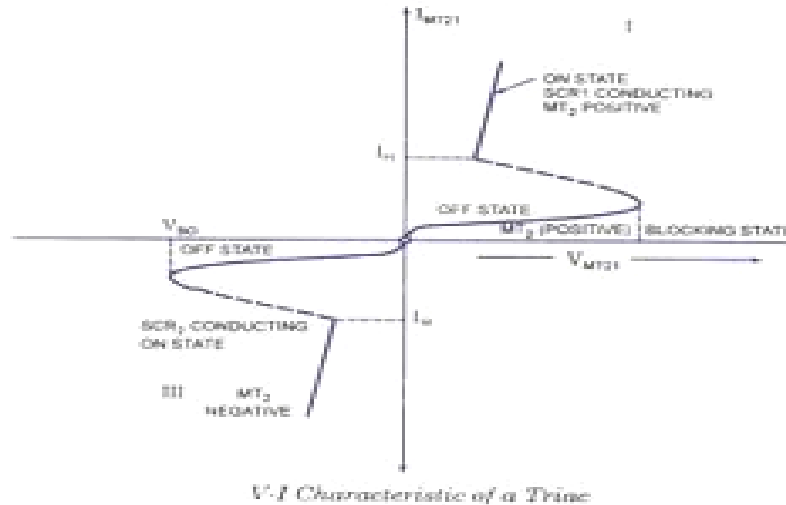
The bidirectionality makes TRIACs very convenient switches for alternating current circuits, also allowing them to control very large power flows with milliampere-scale gate currents. In addition, applying a trigger pulse at a controlled phase angle in an A.C. cycle allows control of the percentage of current that flows through the TRIAC to the load (phase control), which is commonly used, for example, in controlling the speed of low-power induction motors, in dimming lamps, and in controlling A.C. heating resistors.

In quadrants 1 and 2, MT2 is positive, and current flows from MT2 to MT1 through P, N, P and N layers. The N region attached to MT2 does not participate significantly. In quadrants 3 and 4, MT2 is negative, and current flows from MT1 to MT2, also through P, N, P and N layers. The N region attached to MT2 is active, but the N region attached to MT1 only participates in the initial triggering, not the bulk current flow.

In most applications, the gate current comes from MT2, so quadrants 1 and 3 are the only operating modes.

TRIAC Characteristics

Typical V-I characteristics of a triac are shown in figure. The triac has on and off state characteristics similar to SCR but now the characteristic is applicable to both positive and negative voltages. This is expected because triac consists of two SCRs connected in parallel but opposite in directions.



MT_2 is positive with respect to MT_1 in the first quadrant and it is negative in the third quadrant. As already said in previous blog posts, the gate triggering may occur in any of the following four modes.

Quadrant I operation: V_{MT2} , positive; V_{G1} positive

Quadrant II operation: V_{MT2} positive; V_{G1} negative

Quadrant III operation: V_{MT2} negative; V_{G1} negative

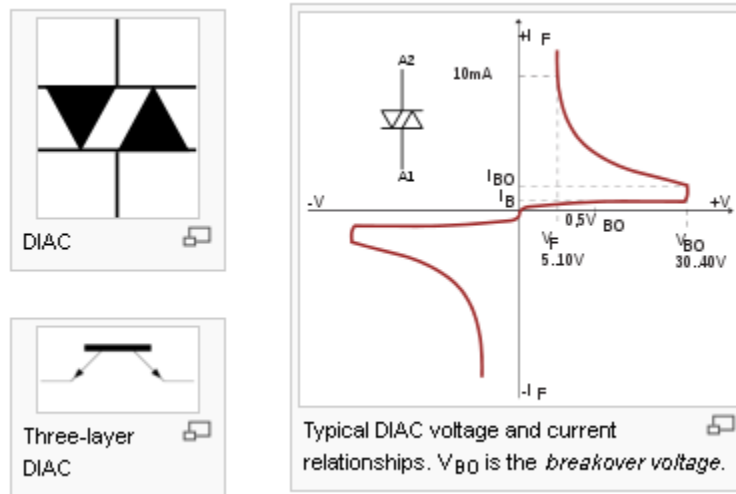
Quadrant IV operation: V_{MT2} negative; V_{G1} positive

where V_{MT2} and V_{G1} are the voltages of terminal MT_2 and gate with respect to terminal MT_1 .

The device, when starts conduction permits a very heavy amount of current to flow through it. This large inrush of current must be restricted by employing external resistance, otherwise the device may get damaged.

The gate is the control terminal of the device. By applying proper signal to the gate, the firing angle of the device can be controlled. The circuits used in the gate for triggering the device are called the gate-triggering circuits. The gate-triggering circuits for the triac are almost same like those used for SCRs. These triggering circuits usually generate trigger pulses for firing the device. The trigger pulse should be of sufficient magnitude and duration so that firing of the device is assured. Usually, a duration of 35 μs is sufficient for sustaining the firing of the device.

DIAC Characteristics:



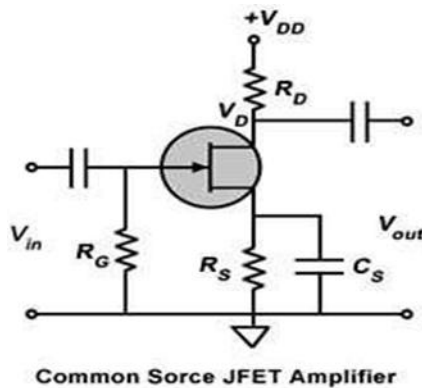
The **DIAC**, or "diode for alternating current", is a diode that conducts current only after its breakover voltage, V_{BO} , has been reached momentarily. When this occurs, the diode enters the region of negative dynamic resistance, leading to a decrease in the voltage drop across the diode and, usually, a sharp increase in current through the diode. The diode remains "in conduction" until the current through it drops below a value characteristic for the device, called the holding current, I_H . Below this value, the diode switches back to its high-resistance (non-conducting) state. This behavior is bidirectional, meaning typically the same for both directions of current. Most DIACs have a three-layer structure with breakover voltage around 30 V. Their behavior is somewhat similar to that of a neon lamp, but it is much more precisely controlled and takes place at a lower voltage. DIACs have no gate electrode, unlike some other thyristors that they are commonly used to trigger, such as TRIACs. Some TRIACs, like Quadrac, contain a built-in DIAC in series with the TRIAC's "gate" terminal for this purpose. DIACs are also called *symmetrical trigger diodes* due to the symmetry of their characteristic curve. Because DIACs are bidirectional devices, their terminals are not labeled as *anode* and *cathode* but as A1 and A2 or MT1 ("Main Terminal") and MT2.

9. Draw the circuit of FET amplifier & explain its operation. (AUC NOV 2011)

Common Source JFET Amplifier

small signal amplifiers can also be made using **Field Effect Transistors** or **FET's**.

These devices have the advantage over bipolar transistors of having extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals. The design of an amplifier circuit based around a junction field effect transistor or "JFET", (n-channel FET) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit. Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. The **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design. The common source JFET amplifier circuit is shown below.



The amplifier circuit consists of an N-channel JFET, connected in a common source configuration. The JFET gate voltage V_g is biased through the potential divider network set up by resistors R_1 and R_2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor. Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing arrangement as long as a steady current flow through the JFET even when there is no input signal present and V_g maintains a reverse bias of the gate-source pn junction. In this example the biasing is provided from a potential divider network

allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal. Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage V_g .

The input signal, (V_{in}) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage V_g applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, R_d . The output voltage, V_{out} is developed across this load resistance. The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, R_s included in the source lead with the same drain current flowing through this resistor. Resistor, R_s is also used to set the JFET amplifiers "Q-point".

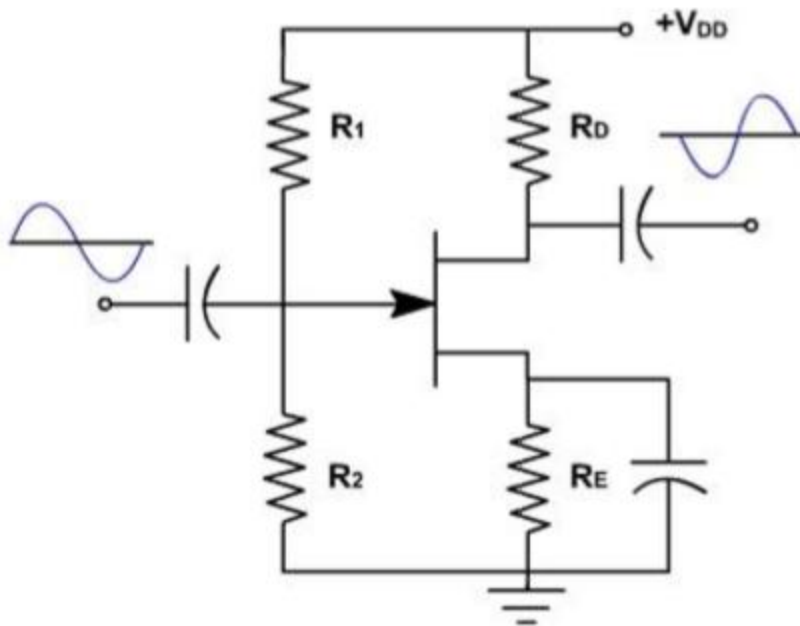
When the JFET is switched fully "ON" a voltage drop equal to $R_s \times I_d$ is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across R_s due to the drain current provides the necessary reverse biasing condition across the gate resistor, R_2 effectively generating negative feedback. In order to keep the gate-source junction reverse biased, the source voltage, V_s needs to be higher than the gate voltage, V_g . This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, I_d is also equal to the Source current, I_s as "No Current" enters the Gate terminal and this can be given as:

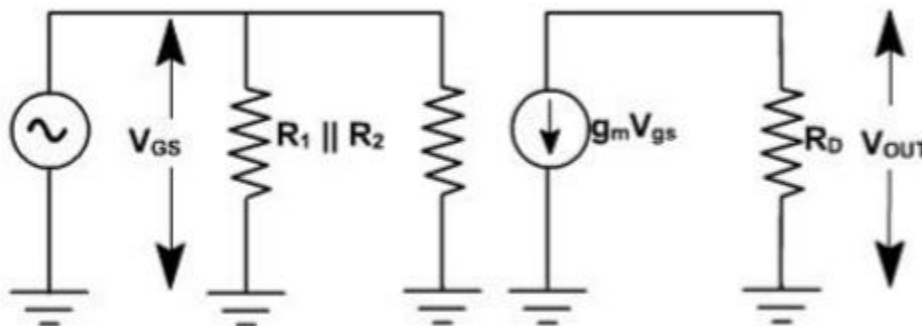
$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, R_s and the source by-pass capacitor, C_s serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across R_s .



When a small ac signal is coupled into the gate it produces variations in gate source voltage. This produces a sinusoidal drain current. Since an ac current flows through the drain resistor. An amplified ac voltage is obtained at the output. An increase in gate source voltage produces more drain current, which means that the drain voltage is decreasing. Since the positive half cycle of input voltage produces the negative half cycle of output voltage, we get phase inversion in a CS amplifier.

The ac equivalent circuit is shown



The ac output voltage is

$$V_{out} = -g_m * V_{gs} * R_D$$

Negative sign means phase inversion. Because the ac source is directly connected between the gate source terminals therefore ac input voltage equals

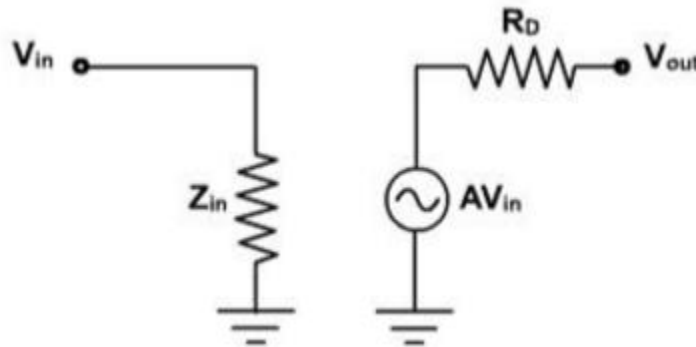
$$V_{in} = V_{gs}$$

The voltage gain is given by

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D$$

$$A_v = \text{unloaded voltage gain}$$

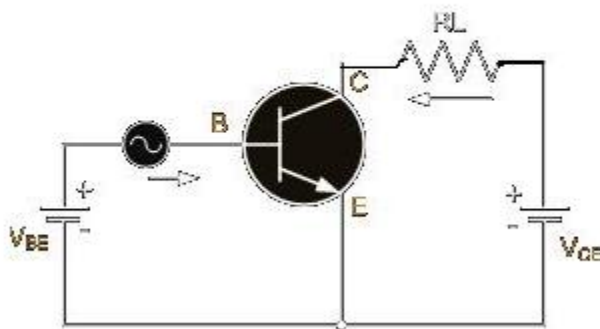
The further simplified model of the amplifier is shown



Z_{in} is the input impedance. At low frequencies, this is parallel combination of $R_1 || R_2 || R_{GS}$. Since R_{GS} is very large, it is parallel combination of R_1 & R_2 . V_{in} is output voltage and R_D is the output impedance.

10. Sketch the input & output characteristics of CE configuration & explain how these are obtained. (AUC NOV 2011)

The Common Emitter Amplifier Circuit

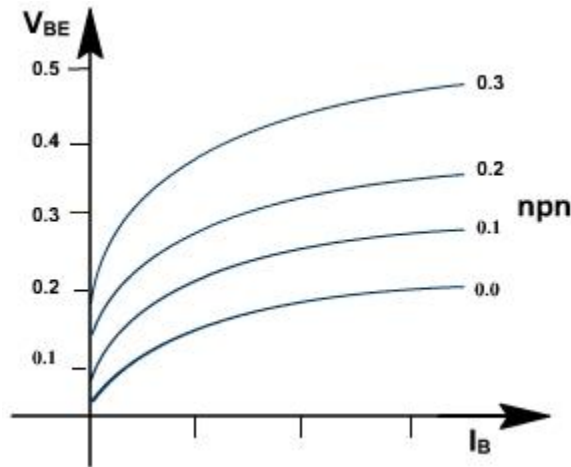


The curves representing the relation between different DC currents and voltages of a transistor helps in studying the operation of a transistor, when they are connected in a circuit. The three important characteristics of a transistor are,

- Input characteristics
- Output characteristics
- Constant current characteristics

Input Characteristics:

I_B varies with V_{BE} when V_{CE} is held constant. V_{BE} is varied and the corresponding variation in I_B is noted. This characteristic curve is used to find the input resistance of a transistor. $R_{in} = (\Delta V_{BE} / \Delta I_B)$ when V_{CE} constant.



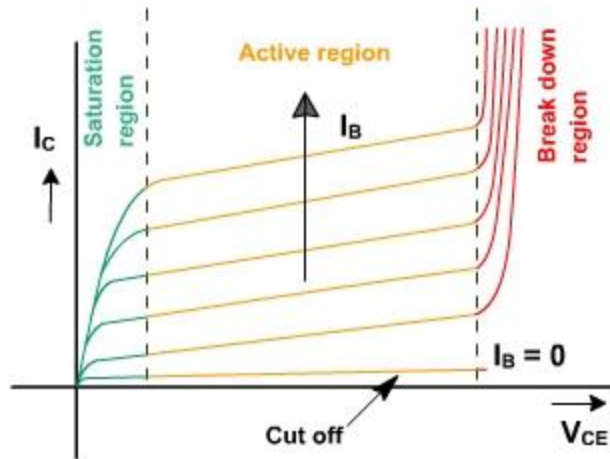
Output Characteristics:

Here I_C varies with V_{CE} when I_B is held constant. V_{CE} is varied when I_B is constant in steps and the corresponding value of I_C is noted. Next V_{CE} is reduced back to zero and I_B is increased to a little higher value than before and the whole procedure is repeated to get the family of curves as shown.

This characteristic is used to find output resistance of a transistor.

$R_{out} = (\Delta V_{CE} / \Delta I_C)$ when I_B is constant.

It can be seen that even when I_B is zero I_C flows in very small amount and this is called leakage current flowing due to the minority charge carriers in reverse biased junction. I_C depends on V_{CE} . If V_{CE} is increased beyond certain value, I_C increases rapidly due to avalanche breakdown.



(1) Active Region:

In this region collector junction is reverse biased and emitter junction is forward biased. It is the area to the right of $V_{CE} = 0.5$ V and above $I_B = 0$. In this region transistor current responds most sensitively to I_B . If transistor is to be used as an amplifier, it must operate in this region.

$$I_E = I_C + I_B$$

$$\text{Since, } I_C = I_{C0} + \alpha_{dc} I_E$$

$$I_C = I_{C0} + \alpha_{dc} (I_C + I_B)$$

$$\text{or } (1 - \alpha_{dc}) I_C = \alpha_{dc} I_B + I_{C0}$$

$$\text{or } I_C = \left(\frac{\alpha_{dc}}{1 - \alpha_{dc}} \right) I_B + \left(\frac{1}{1 - \alpha_{dc}} \right) I_{C0}$$

$$\text{Let, } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

$$\therefore I_C = (1 + \beta_{dc}) I_{C0} + \beta_{dc} I_B$$

β_{dc} is defined as current gain of the transistor is given by

$$\beta_{dc} = \frac{I_C - I_{C0}}{I_B + I_{C0}}$$

If α_{dc} is truly constant then I_C would be independent of V_{CE} . But because of early effect, α_{dc} increases by 0.1% (0.001) e.g. from 0.995 to 0.996 as V_{CE} increases from a few volts to 10V. Then β_{dc} increases from $0.995 / (1 - 0.995) = 200$ to $0.996 / (1 - 0.996) = 250$ or about 25%. This shows that small change in α reflects large change in β . Therefore the curves are subjected to large variations for the same type of transistors.

(2) Cut Off:

Cut off in a transistor is given by $I_B = 0$, $I_C = I_{CO}$. A transistor is not at cut off if the base current is simply reduced to zero (open circuited) under this condition,

$$I_C = I_E = I_{CO} / (1 - \alpha_{dc}) = I_{CEO}$$

The actual collector current with base open is designated as I_{CEO} . Since even in the neighborhood of cut off, α_{dc} may be as large as 0.9 for Ge, then $I_C = 10 I_{CO}$ (approximately), at zero base current. Accordingly in order to cut off transistor it is not enough to reduce I_B to zero, but it is necessary to reverse bias the emitter junction slightly. It is found that reverse voltage of 0.1 V is sufficient for cut off a transistor. In Si, the α_{dc} is very nearly equal to zero, therefore, $I_C = I_{CO}$. Hence even with $I_B = 0$, $I_C = I_E = I_{CO}$ so that transistor is very close to cut off.

In summary, cut off means $I_E = 0$, $I_C = I_{CO}$, $I_B = -I_C = -I_{CO}$, and V_{BE} is a reverse voltage whose magnitude is of the order of 0.1 V for Ge and 0 V for Si.

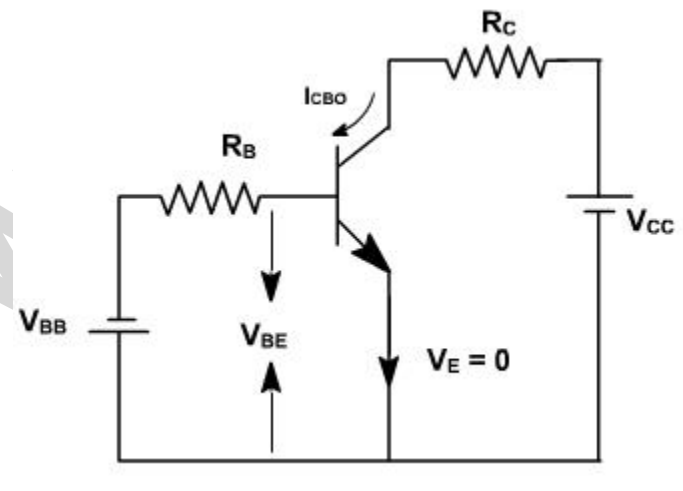
Reverse Collector Saturation Current I_{CBO} :

When in a physical transistor emitter current is reduced to zero, then the collector current is known as I_{CBO} (approximately equal to I_{CO}). Reverse collector saturation current I_{CBO} also varies with temperature, avalanche multiplication and variability from sample to sample. Consider the circuit shown in below figure. V_{BB} is the reverse voltage applied to reduce the emitter current to zero.

$$I_E = 0, \quad I_B = -I_{CBO}$$

If we require, $V_{BE} = -0.1$ V

$$\text{Then } -V_{BB} + I_{CBO} R_B < -0.1 \text{ V}$$



(3). Saturation Region:

In this region both the diodes are forward biased by at least cut in voltage. Since the voltage V_{BE} and V_{BC} across a forward is approximately 0.7 V therefore, $V_{CE} = V_{CB} + V_{BE} = -V_{BC} + V_{BE}$ is also few tenths of volts. Hence saturation region is very close to zero voltage axis, where all the current rapidly reduces to zero. In this region the transistor collector current is approximately given by V_{CC} / R_C and independent of base current. Normal transistor action is lost and it acts like a small ohmic resistance.

Current Transfer characteristics.

Here I_C varies with I_B and V_{CE} is held constant. First V_{CE} is set to a convenient value & I_B is increased in steps & corresponding values of I_C is noted.

Large Signal Current Gain β_{dc} :-

The ratio I_C / I_B is defined as transfer ratio or large signal current gain β_{dc}

$$\beta_{dc} = \frac{I_C}{I_B}$$

Where I_C is the collector current and I_B is the base current. The β_{dc} is an indication of how well the transistor works. The typical value of β_{dc} varies from 50 to 300.

In terms of h parameters, β_{dc} is known as dc current gain and is designated h_{FE} ($\beta_{dc} = h_{FE}$). Knowing the maximum collector current and β_{dc} the minimum base current can be found which will be needed to saturate the transistor.

$$I_{C(max)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = I_{C(sat)}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

This expression of β_{dc} is defined neglecting reverse leakage current (I_{CO}).

Taking reverse leakage current (I_{CO}) into account, the expression for the β_{dc} can be obtained as follows:

β_{dc} in terms of α_{dc} is given by

$$\begin{aligned} \beta_{dc} &= \frac{\alpha_{dc}}{1 - \alpha_{dc}} \\ &= \frac{\frac{I_C - I_{CO}}{I_E}}{1 - \frac{I_C - I_{CO}}{I_E}} = \frac{I_C - I_{CO}}{I_E - I_C + I_{CO}} \\ &= \frac{I_C - I_{CO}}{I_B + I_{CO}} \end{aligned}$$

Since, $I_{CO} = I_{CBO}$

$$\therefore \beta_{dc} = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$$

Cut off of a transistor means $I_E = 0$, then $I_C = I_{CBO}$ and $I_B = -I_{CBO}$. Therefore, the above expression β_{dc} gives the collector current increment to the base current change from cut off to I_B and hence it represents the large signal current gain of all common emitter transistor.

usually β_{dc} is found from the output characteristics rather than from transfer characteristics.

QUESTION BANK

DEPARTMENT: ME

YR/ SEM:II/ III

SUB CODE: ME2255

SUB NAME: ELECTRONICS

& MICROPROCESSORS

UNIT 2-DIGITAL ELECTRONICS

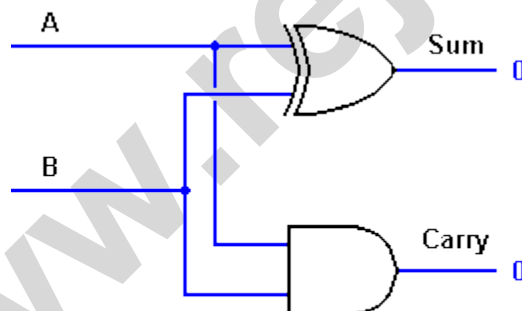
PART A (2 Marks)

1. What are flip flops(AUC MAY 2012)

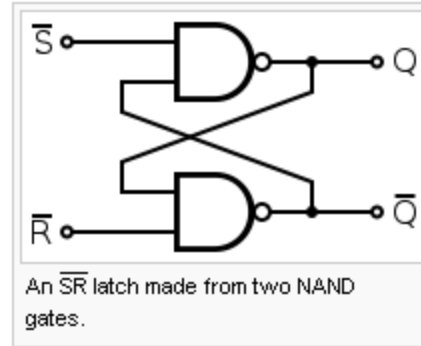
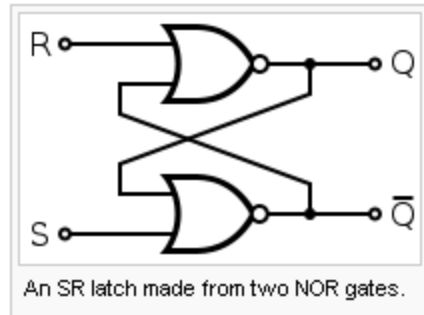
A flip flop is a one bit memory device. This basic digital memory circuit is called flip flop. it is a bistable circuit that has two stable states. Various types of flip flops are,

- RS flip flop
- D flip flop
- T flip flop
- JK flip flop

2. Draw the half adder circuit. (AUC MAY 2012)



3. Draw the circuit of transparent latch.(AUC MAY 2011)



4. Give the truth table & symbolic representation of NAND and NOR. (AUC NOV 2010)

NOR gate

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



NAND gate

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



5. What are universal gates? (AUC NOV 2011)

NAND & NOR gates are called as universal gates.

6. State Demorgans theorem. (AUC NOV 2011)

Theorem 1 : The compliment of a product is equal to the sum of the compliments.

$$\overline{AB} = A'' + B''$$

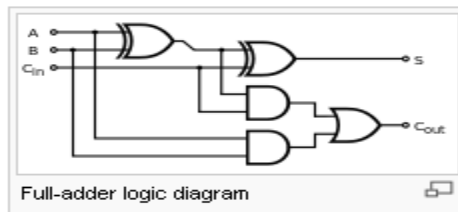
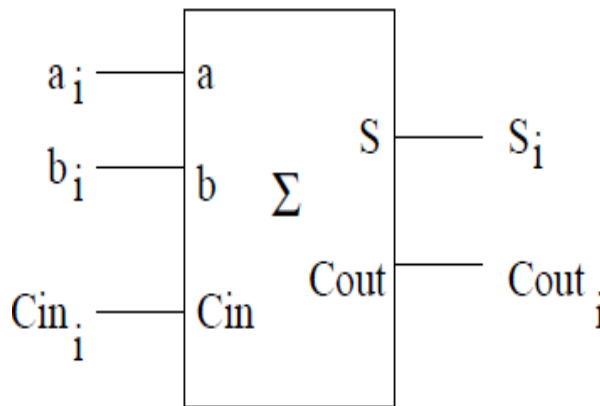
Theorem 2 : The compliment of a sum is equal to the product of the compliments.

$$\overline{A+B} = A'' . B''$$

PART B (8,16 Marks)

1. Design a full adder (AUC MAY 2012, NOV 2011).

The diagram below shows a full adder circuit. It is called full" because it will include a \carry-in" bit and a \carry-out" bit. The carry bits will allow a succession of 1-bit full adders to be used to add binary numbers of arbitrary length. (A *half adder* includes only one carry bit.)



The scheme for the full adder is outlined in Fig. 7. Imagine that we are adding two n -bit binary numbers. Let the inputs a_i and b_i be the i -th bits of the two numbers. The carry in bit Cin_i represents any carry from the sum of the neighboring less significant bits at position $i - 1$. That is, $Cin_i = 1$ if $a_{i-1} = b_{i-1} = 1$, and is 0 otherwise. The sum S_i at position i is therefore the sum of a_i , b_i , and Cin_i . (Note that this is an arithmetic sum, *not* a Boolean OR.) A carry for this sum sets the carry out bit, $Cout_i = 1$, which then can be applied to the sum of the $i + 1$ bits. The truth table is given below.

Cin_i	a_i	b_i	S_i	$Cout_i$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

With $Cin_i = 0$, we see that the output sum S_i is just given by the XOR operation, $a_i \oplus b_i$. And with $Cin_i = 1$, then $S_i = \overline{a_i \oplus b_i}$. Perhaps the simplest way to express this relationship is the following:

$$S_i = Cin_i \oplus (a_i \oplus b_i)$$

To determine a relatively simple expression for $Cout_i$, we will use a K-map:

$Cin_i \backslash a_i b_i$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

This yields

$$Cout_i = a_i b_i + Cin_i a_i + Cin_i b_i = a_i b_i + Cin_i (a_i + b_i)$$

which in hardware would be 2 2-input OR gates and 2 2-input AND gates.

As stated above, the carry bits allow our adder to be expanded to add any number of bits. As an example, a 4-bit adder circuit is depicted in Fig. 8. The sum can be 5 bits, where the MSB is formed by the final carry out. (Sometimes this is referred to as an “overflow” bit.)

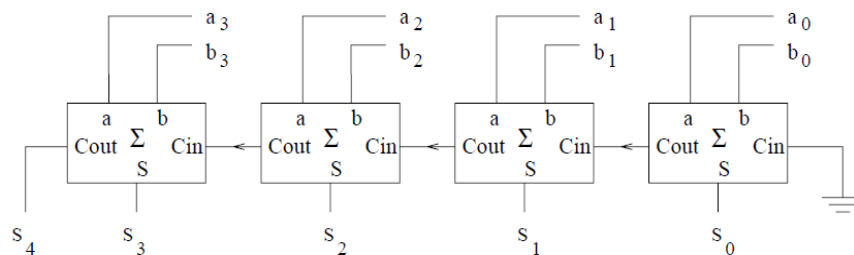


Figure 8: Expansion of 1-bit full adder to make a 4-bit adder.

2. Discuss the operation of RS flip flop and D flip flop. (AUC MAY 2012)

The following 3 figures are equivalent representations of a simple circuit. In general these are called flip-flops. Specifically, these examples are called SR (set-reset) flip-flops, or SR latches.

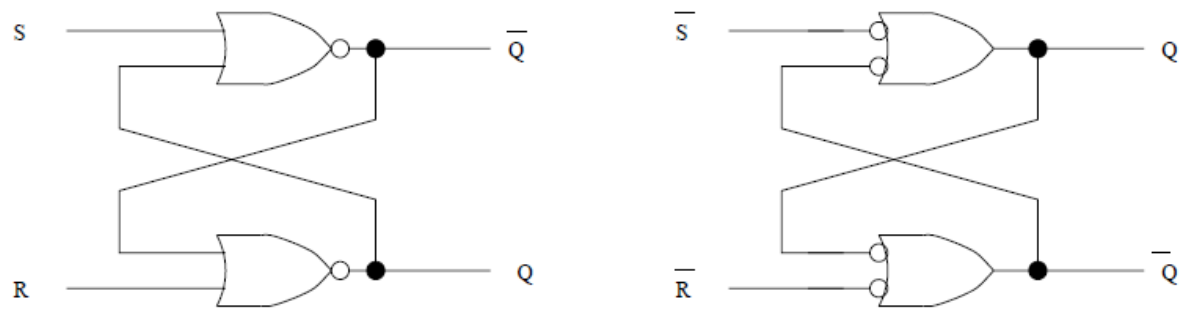


Figure 11: Two equivalent versions of an SR flip-flop (or “SR latch”).

D Flip Flop:

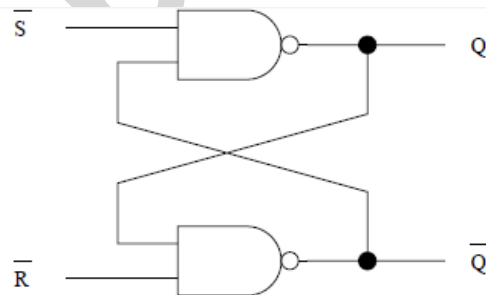


Figure 12: Yet another equivalent SR flip-flop, as used in Lab 3.

The truth table for the SR latch is given below.

S	\bar{S}	R	\bar{R}	Q	\bar{Q}
1	0	0	1	1	0
0	1	1	0	0	1
0	1	0	1	retains previous	
1	0	1	0	0	0

The state described by the last row is clearly problematic, since Q and \bar{Q} should not be the same value. Thus, the $S = R = 1$ inputs should be avoided.

From the truth table, we can develop a sequence such as the following:

1. $R = 0, S = 1 \Rightarrow Q = 1$ (set)
2. $R = 0, S = 0 \Rightarrow Q = 1$ ($Q = 1$ state retained: "memory")
3. $R = 1, S = 0 \Rightarrow Q = 0$ (reset)
4. $R = 0, S = 0 \Rightarrow Q = 0$ ($Q = 0$ state retained)

In alternative language, the first operation "writes" a true state into one bit of memory. It can subsequently be "read" until it is erased by the reset operation of the third line.

clock is a continuous sequence of square wave pulses. There are a number of reasons for the importance of the clock. Clearly it is essential for doing any kind of counting or timing operation. But, its most important role is in providing *synchronization* to the digital circuit. Each clock pulse may represent the transition to a new digital state of a so-called "state machine" (simple processor) we will soon encounter. Or a clock pulse may correspond to the movement of a bit of data from one location in memory to another. A digital circuit coordinates these various functions by the synchronization provided by a single clock signal which is shared throughout the circuit. A more sophisticated example of this concept is the clock of a computer, which we have come to associate with processing speed (e.g. 330 MHz for typical current generation commercial processors.) We can include a clock signal to our simple SR flip-flop, as shown in Fig. 14. The truth table, given below, follows directly from our previous SR flip-flop, except now we include a label for the n th clock pulse for the inputs and the output. This is because the inputs have no effect unless they coincide with a clock pulse. (Note that a specified clock pulse conventionally refers to a HIGH level.) As indicated in the truth table, the inputs $S_n = R_n = 0$ represent the flip-flop memory state. Significantly, one notes that the interval *between* clock pulses also corresponds to the "retain previous state" of the flip-flop. Hence the information encoded by the one bit of flip-flop memory can only be modified in synchronization with the clock.

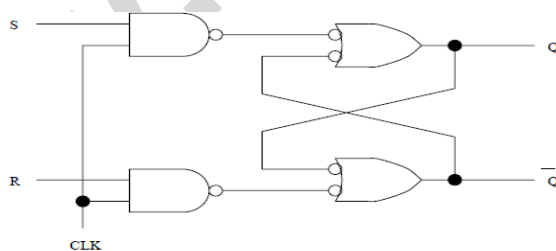


Figure 14: A clocked SR flip-flop.

S_n	R_n	Q_n
1	0	1
0	1	0
0	0	Q_{n-1}
1	1	avoid

We are now set to make a subtle transition for our next version of the clocked flip-flop.

The flip-flop memory is being used to retain the state between clock pulses. In fact, the

state set up by the S and R inputs can be represented by a single input we call "data", or D . This is shown in Fig. 15. Note that we have explicitly eliminated the bad $S = R = 1$ state with this configuration. We can override this data input and clock synchronization scheme by including the "jam set" (S) and "jam reset" (R) inputs shown in Fig. 15. These function just as before with the unlocked SR flip-flop. Note that these "jam" inputs go by various names. So sometimes the set is called "preset" and reset is called "clear", for example.

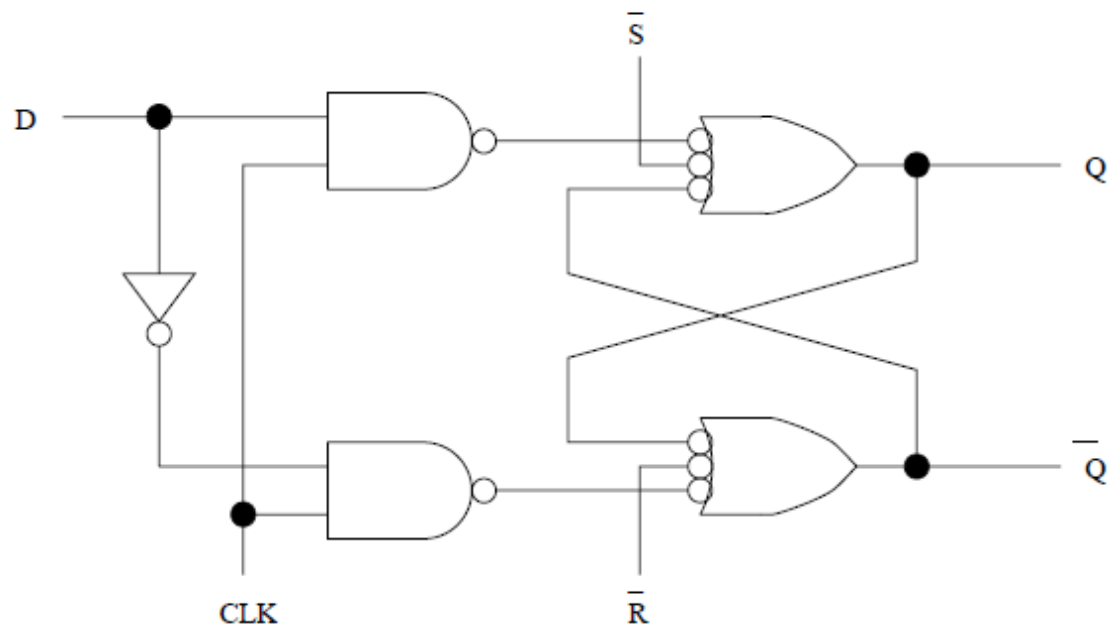
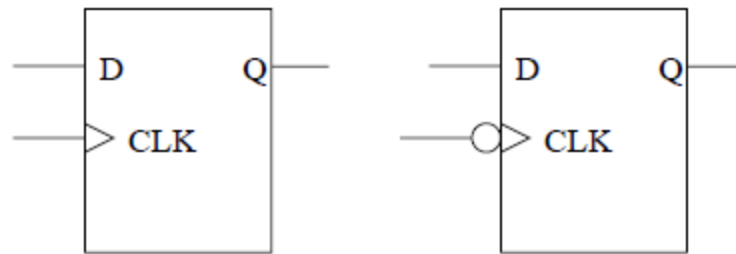


Figure 15: A "D-type transparent" flip-flop with jam set and reset.



A typical timing diagram for this flip-flop is given in Fig. 16. Note that the jam reset signal \bar{R} overrides any action of the data or clock inputs.

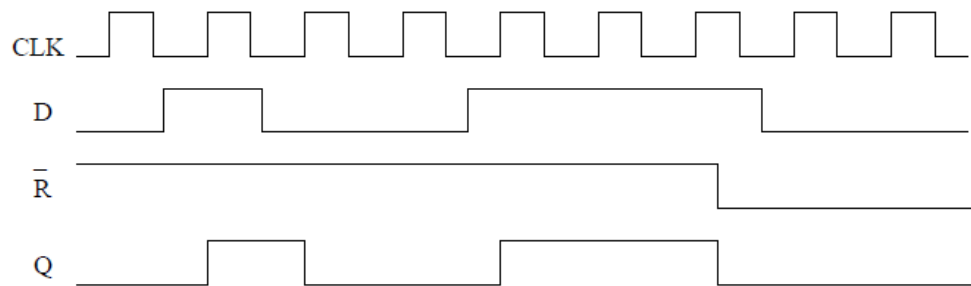


Figure 16: Example of timing diagram for the transparent D flip-flop. (It is assumed that \bar{S} is held HIGH throughout.)

3. Draw & explain the operation of A/D and D/A converters. (AUC MAY 2012)

D/A Conversion

The basic element of a DAC is the simplest analog divider: the resistor. First, we need to review the two important properties of an operational amplifier (op-amp) connected in the inverting configuration. This is shown in Fig. 25. The two important properties are

1. The $-$ input is effectively at ground. (virtual ground")
2. The voltage gain is $G = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$. An equivalent statement is that for a current at the $-$ input of $i_{in} = \frac{V_{in}}{R_1}$, the output voltage is $V_{out} = G V_{in} = -R_2 i_{in} = -V_{in} \frac{R_2}{R_1}$. Sometimes this is written in the form $V_{out} = g i_{in}$, where g is the *transconductance*, and $g = -\frac{R_2}{R_1}$ in this case.

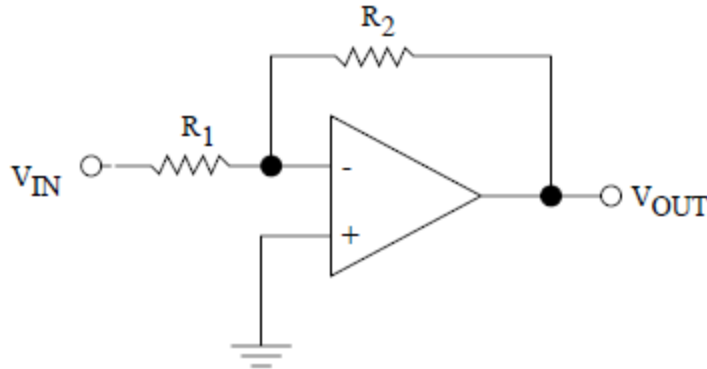


Figure 25: Inverting op-amp configuration.

The basic idea of most DACs is then made clear by the 4-bit example illustrated in Fig. 26. The input 4-bit digital signal defines the position of the switches labelled a_0 – a_3 . A HIGH input bit would correspond to a switch connected to 1.0 V, whereas a LOW connects to ground. The configuration in the figure represents a binary input of 1010, or 10_{10} . Since the virtual ground keeps the op-amp input at ground, then for a switch connected to ground, there can be no current flow. However, for switches connected to 1.0 V, the current presented to the op-amp will be 1.0 V divided by the resistance of that leg. All legs with HIGH switches then contribute some current. With the binary progression of resistance values shown in the figure, the desired result is obtained. So for the example shown, the total current to the op-amp is $I = 1.0/R + 1.0/(4R) = 5/(4R)$. The output voltage is

$$V_{\text{out}} = -RI = 5/4 = 1.25\text{V}$$

When all input bits are HIGH ($1111 = 15_{10}$), we find $V_{\text{out}} = 15/8$ V. A simple check of our scheme shows that

$$(5/4)/(15/8) = 2/3 = 10/15 = 1010/1111$$

as expected.

The R-2R Ladder

This represents a rather minor point, although it is an interesting idea. The “R-2R ladder” is of practical interest because it uses only two resistor values. Since it is difficult to accurately fabricate resistors of arbitrary resistance, this is beneficial. The two resistances of the R-2R

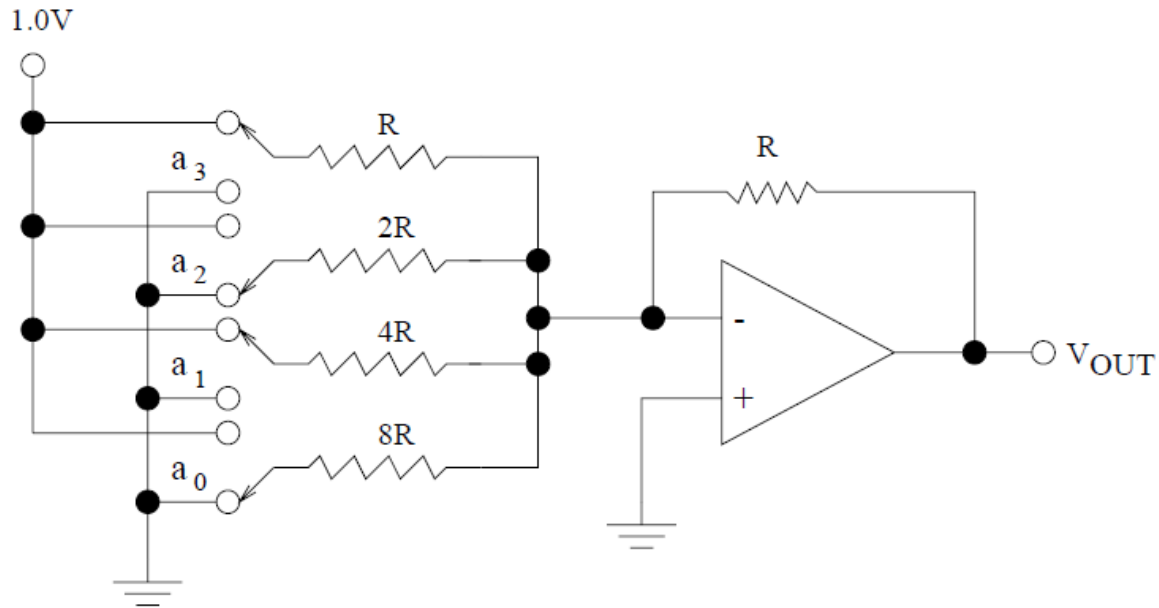


Figure 26: Example 4-bit DAC scheme.

are to be contrasted with the scheme represented by the circuit of Fig. 26, which employs as many resistance values as there are bits. The idea behind the R-2R ladder hinges on noticing the pattern of equivalences represented by Fig. 27, which can be used to replicate an arbitrarily long ladder, and hence handle in arbitrary number of bits.

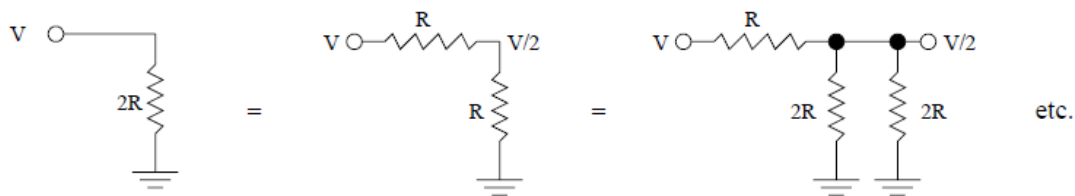


Figure 27: Principle of the R-2R ladder. The rightmost 2R resistor can be indefinitely replicated with this equivalent circuit.

A/D Conversion

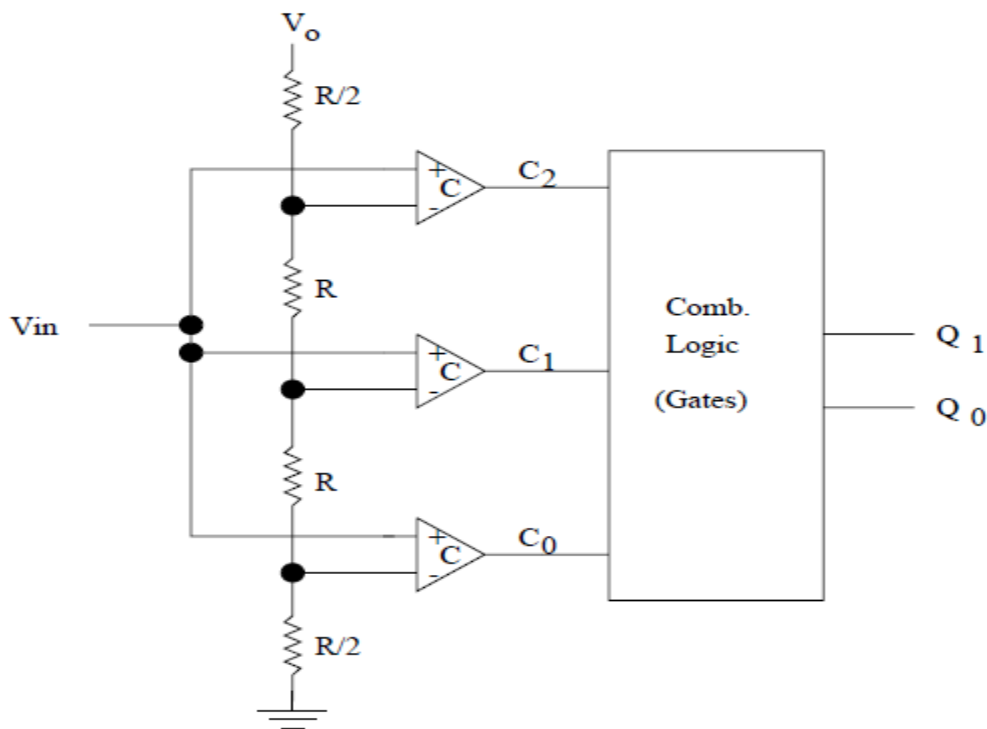
ADCs fall into 3 general types of technique:

- (1) parallel encoding (flash): fast; limited accuracy
- (2) successive approx. (feedback): med. fast; good accuracy
- (3) single or double slope: slow; best potential accuracy

All of these techniques use a device known as a *comparator*. This was discussed in 431/531 and in the text Chapters 4 and 9. Here, we will not discuss how comparators work, but we do need to know what they do. There are many makes of comparators. We will use the model LM311 in lab. Figure 28 shows a comparator schematically. Internally, the comparator can be thought of as a fast, very high-gain differential amplifier (“A”) with inputs “+” and “−.” We can put a “threshold voltage” at the “−” input. Call it V_{th} . The circuit input V_{in} is connected to the “+” input. When $V_{in} > V_{th}$, the comparator amplifies this difference until the output reaches its largest possible value, which is determined by the connection through the pull-up resistor. In the configuration shown here, as well as in Lab 5, the $\sim 1\text{ k}\Omega$ pull-up resistor is connected to +5 V. (Note that while +5 V is convenient for many digital circuits, it is possible to use other values, such as +12 V.) When $V_{in} < V_{th}$, the output swings the other way. This level is usually determined by a connection to one of the comparator pins. Here, it is ground.

Flash ADCs

In this scheme, the input is fanned out in parallel to several comparators with monotonically increasing thresholds. The pattern of comparator outputs is then analyzed by some combinational logic (*i.e.* gates) to determine the output. This technique is called *flash* (or *parallel*) *encoding*. We exemplify the flash ADC scheme with the 2-bit ADC shown in Fig. 29. With $n = 2$ bits, we need to define $2^n = 4$ possible states. These states represent 4 separate intervals. The analog input will fall into one of these intervals, and we will encode this assignment with the 2 bits. Defining the boundaries of 2^n intervals requires $2^n - 1$ comparators, with the threshold of each comparator set to the appropriate boundary voltage.



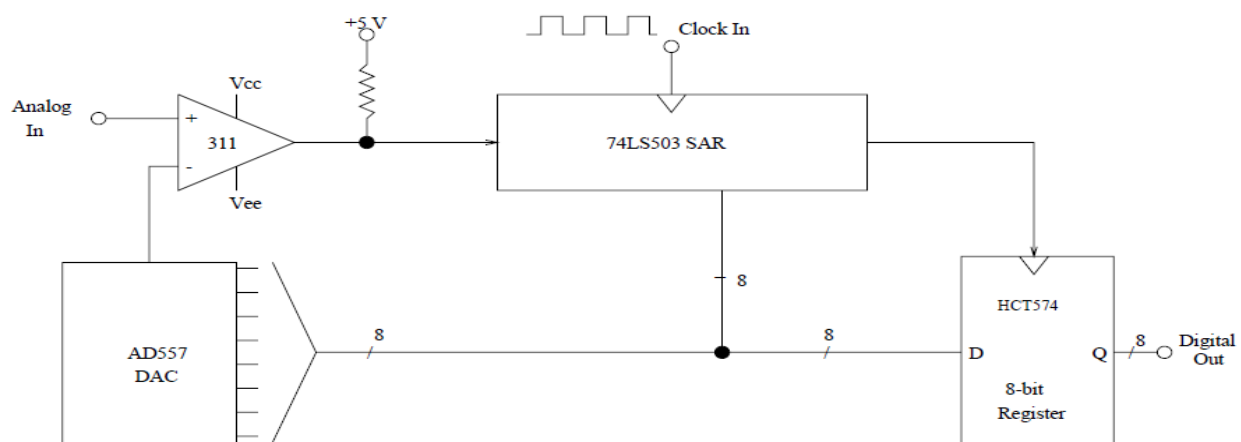
Let's go through a concrete example. Assume that our FADC circuit is designed to handle analog voltage input signals in the range -0.5 to 3.5 V. Thus, we have a 4-volt total input range, with each interval spanning 1.0 V. Therefore, each state will have a maximum error, or resolution, of half the interval, or 0.5 V. (This is $4.0/(2 \cdot 2^n)$, as we said previously in our definition of resolution.) So an input which is in the range 2.5 – 3.5 V will give a HIGH output only to comparator output C_2 , and our digital estimation will correspond to 3.0 V. Hence, the threshold for the upper comparator (its “–” input) should be set at 2.5 V. Similarly for the remaining comparators we work out the values which are given in the table below, where V_{est} is the digital estimate which corresponds to each state.

V_{in} range	Comparator	Threshold	V_{est}	$C_2C_1C_0$	Q_1Q_0
2.5 – 3.5 V	C_2	2.5 V	3.0 V	111	11
1.5 – 2.5 V	C_1	1.5 V	2.0 V	110	10
0.5 – 1.5 V	C_0	0.5 V	1.0 V	100	01
-0.5 – 0.5 V	–	–	0.0 V	000	00

Using Ohm's and Kirchoff's Laws, we arrive at the resistance ratios shown in Fig. 29 in order to achieve the desired comparator thresholds. All that remains is to determine the gate logic to convert the pattern of comparator outputs to a 2-bit digital output. Generalizing from the above, we see that we have agreement with our previous statements: For an n -bit ADC, we require $2^n - 1$ comparators, and the resolution is $\Delta V/2^{n+1}$, where ΔV is the full range of analog input.

Successive Approximation ADCs

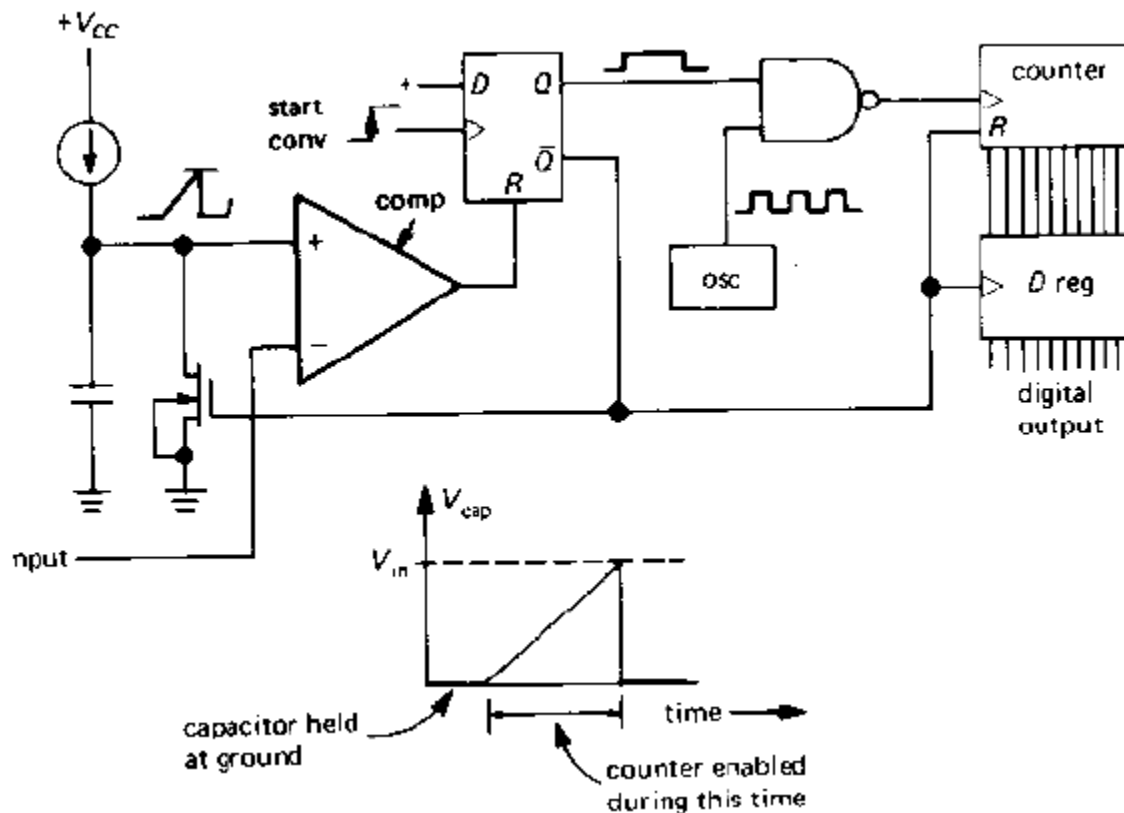
This technique is illustrated by Fig. 30, which is also the one given for Lab 5. It uses a digital feedback loop which iterates once on successive clock cycles. The function of the *successive approximation register*, or SAR, is to make a digital estimate of the analog input based on the 1-bit output of the comparator. The current SAR estimate is then converted back to analog by the DAC and compared with the input. The cycle repeats until the “best” estimate is achieved. When that occurs, this present best estimate is latched into the output register (written into memory). By far the most common algorithm employed by SARs is the *binary search algorithm*.



Single/Dual Slope ADCs

These techniques are slower than flash or successive approximation, but in principle can be quite accurate. The improved accuracy is for two reasons, because time, which is robustly measured using digital techniques, is used as the measured quantity, and because there is some immunity to noise pickup, especially for the dual slope case.

The single slope technique is illustrated in Fig. 32, which is taken from Figure 9.54 of the text. The device near the input and the capacitor is an FET transistor which is used as a switch. When the input to the FET gate, which comes from the \bar{Q} output of the D-type flip-flop, is LOW, then the FET is switched off, and it draws no current. However, when \bar{Q} goes HIGH, the FET pulls the + input of the comparator to ground, and holds it there. The box marked "osc" represents a typical digital clock. The arrow within the circle connected to $+V_{cc}$ is the symbol for a "current source", which means that its output is a constant current, regardless of the impedance at its output (within reasonable bounds).



The process begins when a rising-edge signal is sent to the flip-flop, for example from a debounced switch. Since the D input is HIGH, then Q goes HIGH. Hence the counter, no longer being held at reset by the flip-flop, begins counting. At the same time the FET is

switched off and a signal is sent to the $-$ input of the comparator. Now we must analyze the nature of this signal.

The voltage across a capacitor V_{cap} , is related to its stored charge by $V_{\text{cap}} = Q/C$, where C is the capacitance. Differentiating gives $dV_C/dt = I/C$. Now, because of the current source, the right-hand side of this equation is a constant. Finally, since one side of the capacitor is at ground, then the comparator $+$ input is just V_{cap} . Hence, we can integrate our expression over a time interval Δt to give:

$$V_+ = V_{\text{cap}} = (I/C)\Delta t$$

Since I/C is a known constant, this equation allows one to convert the V_+ input to a time Δt to be measured by the counter. This linear relation between V_+ ($= V_{\text{cap}}$) and Δt is illustrated in the figure. The counter stops (is reset) and its final count stored in the register when V_+ becomes equal to V_{in} , thus changing the state of the comparator. This also resets the flip-flop, thus returning the circuit to its initial state.

The dual-slope ADCs work similarly, but with a two-step process. First, a capacitor is charged for a fixed time τ with a current source whose current is proportional to V_{in} , $I = \alpha V_{\text{in}}$, where α is the constant of proportionality. Hence, V_{cap} is proportional to τ : $V_{\text{cap}} = \alpha V_{\text{in}} \tau / C$. The capacitor is then discharged at constant current I' and the time Δt to do so is measured. Therefore,

$$\Delta t = [C/I'] [\alpha \tau / C] V_{\text{in}} = \beta V_{\text{in}}$$

where $\beta = \alpha \tau / I'$ is a known constant.

This technique has two advantages compared with single-slope. First, we see from the equation above that the result is independent of C . This is good, as precise capacitance values are difficult to fabricate. Second, the integration of the input voltage in the charge-up step allows 60 Hz pickup noise (or other periodic noise) to be averaged to zero.

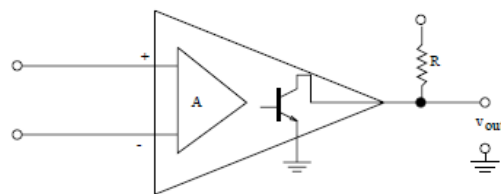
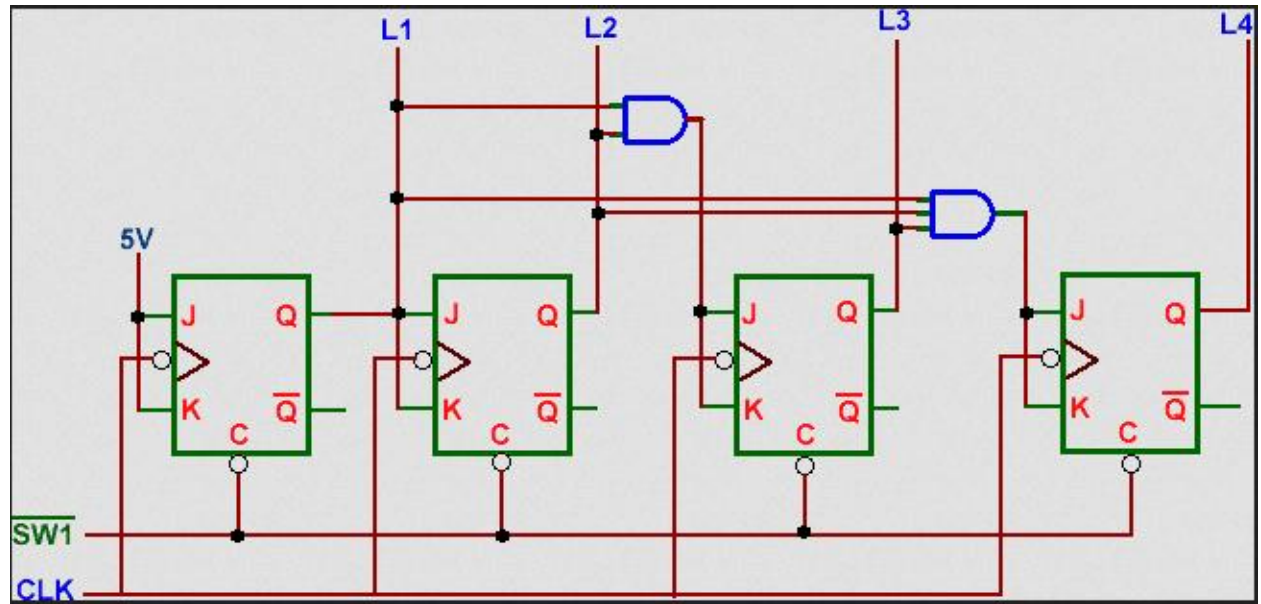


Figure 28: Comparator.

Hence, the comparator represents a one-bit ADC. When the analog input exceeds the pre-defined threshold, the output goes to digital HIGH, and when the input is less than the threshold, the output goes to digital LOW.

4. Implement the full adder circuit from its truth table.(AUC MAY 2010) – same as Q1

5. Design a 4 bit binary parallel counter. Support your answer with circuit diagram & truth table.(AUC MAY 2010)



A 4 bit MOD 16 synchronous counter with parallel carry is shown. In this counter the clock inputs of all the flip flops are connected together so that the input clock signal is applied simultaneously to all flip flops. Also, only the LSB flip flop A has its J & K inputs connected permanently to Vcc while the J & K inputs of the other flip flops are driven by some combination of flip flops outputs. The J & K inputs of the flip flop B are connected with Q_A output of flip flop A; the J & K inputs of flip flop C are connected with AND operated output of Q_A and Q_B ; similarly the J & K inputs of D flip flop are connected with AND operated output of Q_A , Q_B , and Q_C .

STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

According to the truth table, flip flop A changes its state with the occurrence of negative transition at each clock pulse. The flip flop B changes its state when $Q_A=1$ and when there is negative transition at clock input. Flip flop C changes its state when $Q_A=Q_B=1$ and when there is negative transition at clock input. Similarly, D flip flop changes its state when $Q_A=Q_B=Q_C=1$ and when there is negative transition at clock input.

In a parallel counter all flip flops changes its state simultaneously. They are all synchronized with the negative transition of the input clock signal. Thus the total propagation delay is cumulative, the total settling or response time of a synchronous counter is given below.

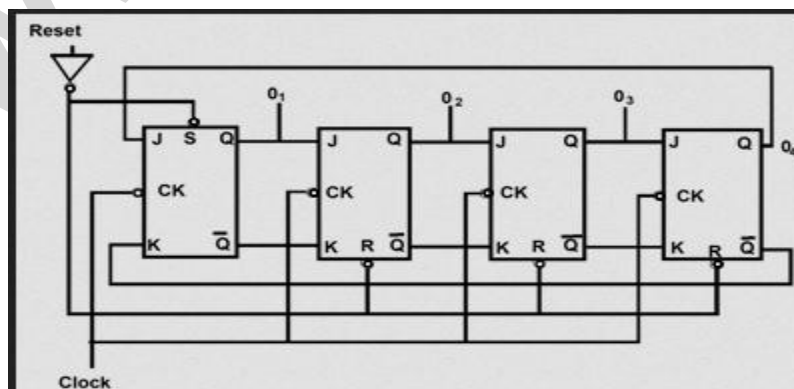
The time taken by one flip flop to toggle plus the time for the new logic levels to propagate through a single AND gate to reach the J & K inputs of the following flip flop

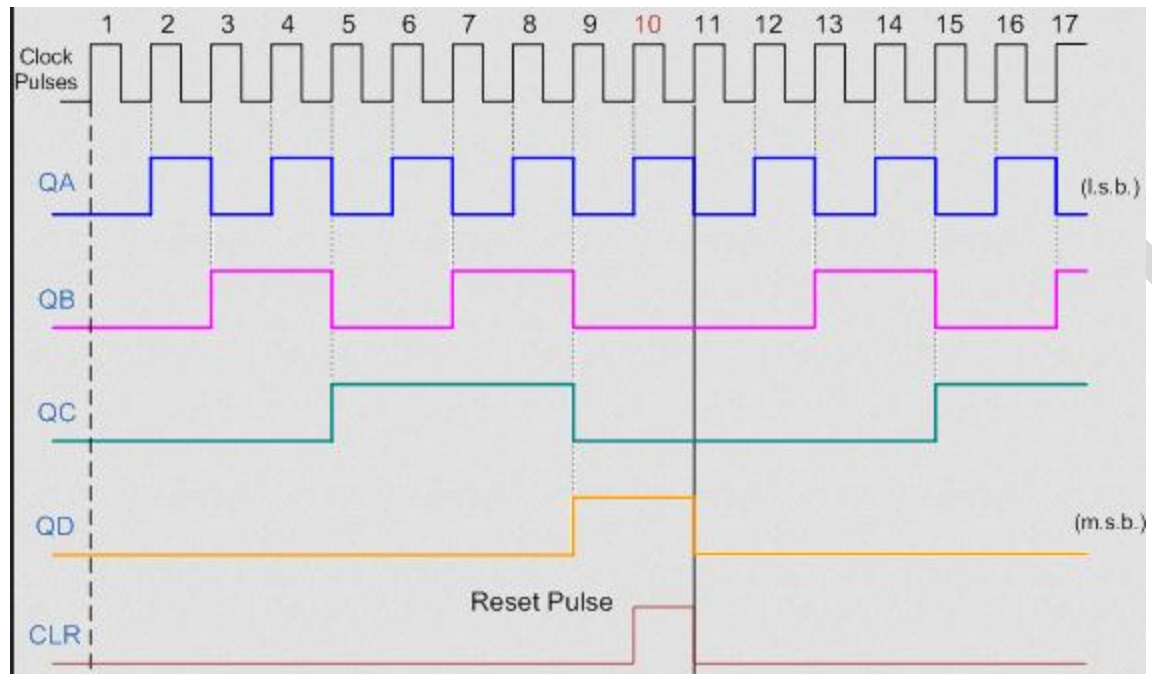
Total delay = propagation delay of one flip flop + propagation delay of AND gate.

The maximum frequency of operation of synchronous counter is given by,

$$F_{\max} = 1/(t_p + t_g)$$

6. With the logic diagram, explain the working of ring counter. Also draw the timing diagram. (AUC MAY 2011)





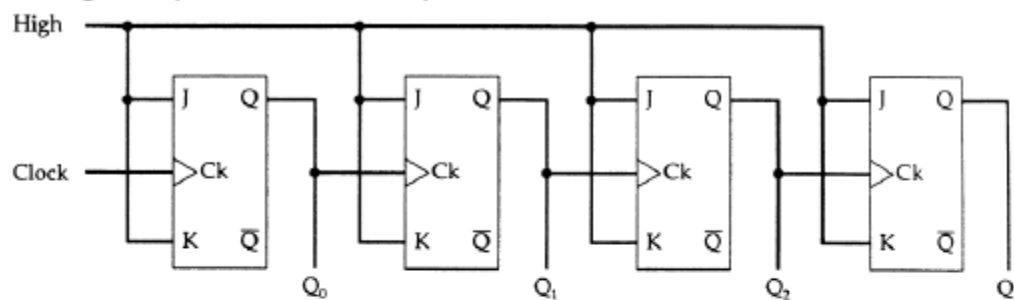
This counter works on the principle of feedback. When we have a state 1 at the last flip flop. On the arrival of the next pulse, this is shifted to first flip flop and this process is repeated on the occurrence of every clock pulse. Therefore 1 circulates around the register as long as clock pulse keeps on arriving. So this counter is called circulating register or ring counter.

The figure shows the circuit of a 4 stage ring counter. It has 4 flip flops a, B, C and D. initially the flip flops are cleared using the Reset pulse. Consider initially the output ABCD= 0001 now $JB+0+JC=JD$ and $KB=KC=KD=1$ while $JA=1$ and $K=0$. Therefore on receipt of the first clock pulse only the flip flop A changes its state from 0 to 1 and other flip flops remain unchanged. So the output is ABCD = 1000

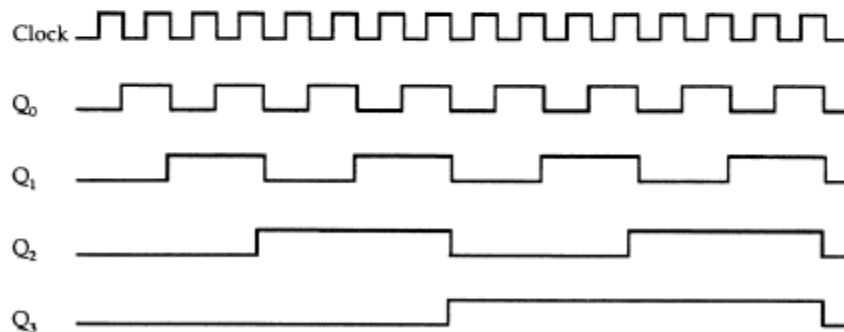
Now $JB=1$ and $KB=0$ and $JA=JC=JD=0$ and $KA=KC=KD=0$. Therefore on the receipt of the second clock pulse only the flip flop B changes from 0 to 1 and other flip flops are not affected. Now the output is ABCD=0100. In this way the 1 keeps on shifting one flip flop to another as long as clock pulse are applied.

Clock pulse	D	C	B	A
0	0	0	0	1
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

- The ring counter is used for counting the number of pulses. Since there is one pulse at output for each of the N clock pulses, this circuit is called a divide by N counter or a N:1 scalar.
7. Design half & Full adder. (AUC NOV 2010)
Same as Q1
8. Explain the successive approximation type of A/D and resistor to ladder D/A converter. (AUC NOV 2010) – same as Q3
9. With the help of neat circuit diagram explain the function of Ripple counter. (AUC NOV 2011)



(a) Sequential Circuit



(b) Timing Diagram

The Asynchronous counter is the simplest in form of logical operations. The clock pulse is applied to the first flip-flop. The successive flip flop is triggered by the output of the previous flip flop & the counter has a cumulative settling time. As the trigger moves through the flip flop like a ripple, it is called ripple counter.

The above figure shows the 4 bit binary ripple counter constructed using JK flip flop. The system clock, a square wave drives the flip flop A. the output of A drives the flip flop B, output of B drives C & output of C drives D. the overall propagation delay time of the counter is the sum of individual delays of flip flops. All the J & K input are connected to Vcc(1), which means that each flip flop toggles on the negative edge of its clock input.

Consider initially all the flip flop to be in logical 0 state (i.e., $Q_A=Q_B=Q_C=Q_D=0$). A negative transition 1 to 0 in the clock input which drives flip flop A causes Q_A to change from logical 0 to logical 1. Flip flop B does not change its state since it also requires a negative transition at its clock input i.e., it requires its clock input Q_A to change from logical 1 to logical 0. This change of state creates the negative going edge needed to trigger flip flop B and thus Q_B goes from 0 to 1. Before the arrival of the sixteenth clock pulse, all the flip flops are in logic 1 state. Clock pulse 16 causes Q_A , Q_B , Q_C and Q_D to go to logical 0 state in turn.

STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

The table shows the sequence of binary states that the flip flops will follow as clock pulses are applied continuously. An n bit binary counter repeats the counting sequence for every 2^n (n is the number of flip flops) clock pulses and has discrete states from 0 to 2^n-1

Mod- Number or Modulus:

The above counter has 16 different states. Thus it is a MOD 16 ripple counter. The MOD number is the total number of states it sequences through in each complete cycle. $\text{MOD number} = 2^n$

QUESTION BANK

DEPARTMENT: ME

YR/ SEM:II/ III

SUB CODE: ME2255

SUB NAME: ELECTRONICS

& MICROPROCESSORS

UNIT 4- 8085 MICROPROCESSOR

PART A (2 Marks)

1. List the various instruction types in 8085.(AUC MAY 2012)

Instruction set of 8085 is classified as

- Data transfer or copy instructions
- Arithmetic instructions
- Logical instructions
- Branching instructions
- Machine Control instructions

2. What are the various addressing modes in 8085? (AUC MAY 2012, NOV 2011)

- Immediate addressing
- Register addressing
- Direct addressing
- Indirect addressing

3. Specify the output at port 1 if the following ALP is executed: (AUC MAY 2010)

MVI B, 88H

MOV A,B

MOV C,A

MVI D, 73H

Out port 1

HLT

4. List the interrupts & call locations. (AUC MAY 2010).

Interrupt	Vector address
RST 0	0000 _H
RST 1	0008 _H
RST 2	0010 _H
RST 3	0018 _H
RST 4	0020 _H
RST 5	0028 _H
RST 6	0030 _H
RST 7	0038 _H

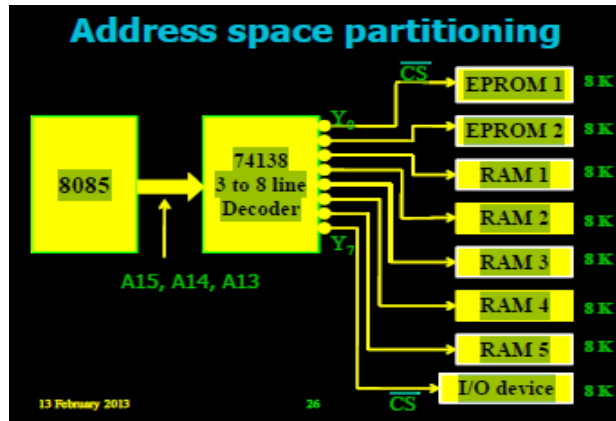
Interrupt	Vector address
RST 7.5	003C _H
RST 6.5	0034 _H
RST 5.5	002C _H
TRAP	0024 _H

5. Name the address partitioning technique used in 8085. (AUC MAY 2011)

Address partitioning techniques is of two types namely,

- Memory mapped I/O
- I/O mapped I.O

The microprocessor has to provide memory for external I/O devices connected. The technique used for allocation of memory for different I/O devices is called memory partitioning. This technique is called memory mapped I/O. Some microprocessors have a single memory where the I/O devices are given the space from the same memory. In some processors a separate memory is provided for I/O devices. This technique is called I/O mapped I/O. consider the below figure for better understanding.



6. What is the output at part 1 when the following instructions are executed? (AUC MAY 2011)

MVI A, 8FH

ADI 72H

JC LOOP

OUT PORT1

HLT

LOOP: XRA A

OUT PORT1

HLT

7. List out the 16 bit registers in 8085. (AUV NOV 2010)

- BC
- DE
- HL
- Program counter
- Stack pointer
- Increment/ Decrement address latch

8. Explain the 8085 instruction DAA. (AUC NOV 2010)

Decimal adjust accumulator

DAA none : The contents of the accumulator are changed from a binary value to two 4-bit binary coded decimal (BCD) digits. This is the only instruction that uses the auxiliary flag to perform the binary to BCD conversion, and the conversion procedure is described below. S, Z, AC, P, CY flags are altered to reflect the results of the operation. If the value of the low-order 4-bits in the accumulator is greater than 9 or if AC flag is set, the instruction adds 6 to the low-order four bits. If the value of the high-

order 4-bits in the accumulator is greater than 9 or if the Carry flag is set, the instruction adds 6 to the high-order four bits.

Example: DAA

9. What do you mean by ALU. (AUC NOV 2011)

Arithmetic and Logic Unit

There is always a need to perform arithmetic operations like +, -, *, / and to perform logical operations like AND, OR, NOT etc. So there is a necessity for creating a separate unit which can perform such types of operations. These operations are performed by the Arithmetic and Logic Unit (ALU). ALU performs these operations on 8-bit data. But these operations cannot be performed unless we have an input (or) data on which the desired operation is to be performed. So from where do these inputs reach the ALU? For this purpose accumulator is used. ALU gets its Input from accumulator and temporary register. After processing the necessary operations, the result is stored back in accumulator.

PART B (8,16 Marks)

1. Sketch the architecture of 8085 & explain the modules in detail.(AUC MAY 2012, NOV2010, MAY 2010, NOV 2011)

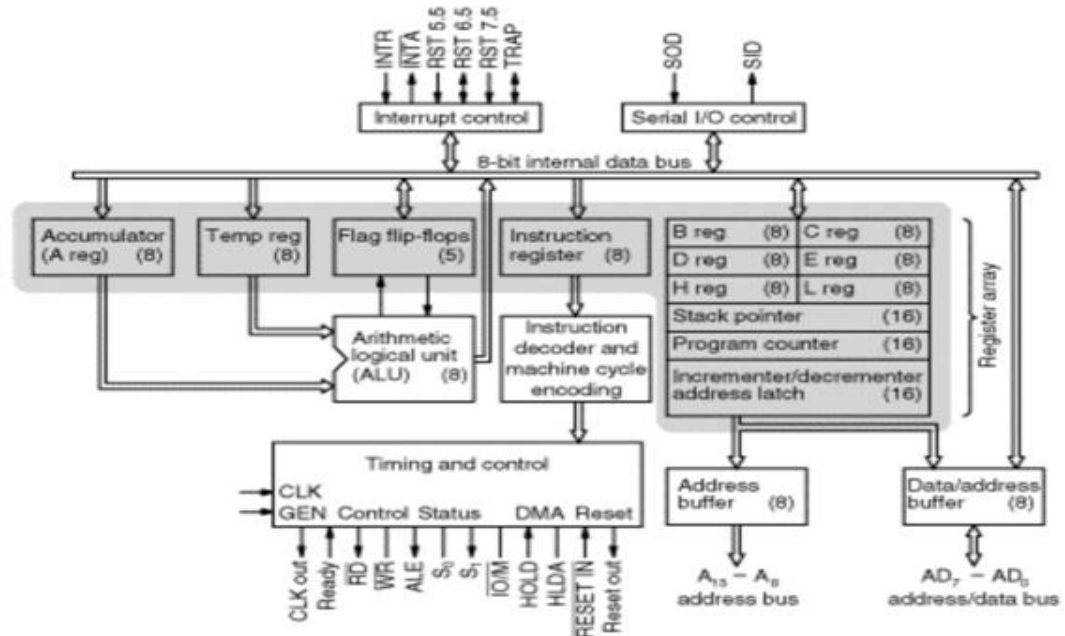
Architecture of 8085 microprocessor

8085 consists of various units and each unit performs its own functions. The various units of a microprocessor are listed below

- Accumulator
- Arithmetic and logic Unit
- General purpose register
- Program counter
- Stack pointer
- Temporary register
- Flags
- Instruction register and Decoder
- Timing and Control unit
- Interrupt control
- Serial Input/output control
- Address buffer and Address-Data buffer
 - Address bus and Data bus

Accumulator

Accumulator is nothing but a register which can hold 8-bit data. Accumulator aids in storing two quantities. The data to be processed by arithmetic and logic unit is stored in accumulator. It also stores the result of the operation carried out by the Arithmetic and Logic unit. The accumulator is also called an 8-bit register. The accumulator is connected to Internal Data bus and ALU (arithmetic and logic unit). The accumulator can be used to send or receive data from the Internal Data bus.



Arithmetic and Logic Unit

There is always a need to perform arithmetic operations like +, -, *, / and to perform logical operations like AND, OR, NOT etc. So there is a necessity for creating a separate unit which can perform such types of operations. These operations are performed by the Arithmetic and Logic Unit (ALU). ALU performs these operations on 8-bit data.

But these operations cannot be performed unless we have an input (or) data on which the desired operation is to be performed. So from where do these inputs reach the ALU? For this purpose accumulator is used. ALU gets its Input from accumulator and temporary register. After processing the necessary operations, the result is stored back in accumulator.

General Purpose Registers

Apart from accumulator 8085 consists of six special types of registers called General Purpose Registers. What do these general purpose registers do? These general purpose registers are used to hold data like any other registers. The general purpose registers in 8085 processors are B, C, D, E, H and L. Each register can hold 8-bit data. Apart from the above function these registers can also be used to work in pairs to hold 16-bit data. They can work in pairs such as B-C, D-E and H-L to store 16-bit data. The H-L pair works as a memory pointer. A memory pointer holds the address of a particular memory location. They can store 16-bit address as they work in pair.

Program Counter and Stack Pointer

Program counter is a special purpose register. Consider that an instruction is being executed by processor. As soon as the ALU finished executing the instruction, the processor looks for the next instruction to be executed. So, there is a necessity for holding the address of the next instruction to be executed in order to save time. This is taken care by the program counter. A program counter stores the address of the next instruction to be executed. In other words the program counter keeps track of the memory address of the instructions that are being executed by the microprocessor and the memory address of the next instruction that is going to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed. Program counter is a 16-bit register. Stack pointer is also a 16-bit register which is used as a memory pointer. A stack is nothing but the portion of RAM (Random access memory). So does that mean the stack pointer points to portion of RAM? Yes. Stack pointer maintains the address of the last byte that is entered into stack. Each time when the data is loaded into stack, Stack pointer gets decremented. Conversely it is incremented when data is retrieved from stack.

Temporary Register:

As the name suggests this register acts as a temporary memory during the arithmetic and logical operations. Unlike other registers, this temporary register can only be accessed by the microprocessor and it is completely inaccessible to programmers. Temporary register is an 8-bit register. In the next article let us discuss about the FLAGS.

Flags

Flags are nothing but a group of individual Flip-flops. The flags are mainly associated with arithmetic and logic operations. The flags will show either a logical (0 or 1) (i.e.) a set or reset depending on the data conditions in accumulator or various other registers. A flag is actually a latch which can hold some bits of information. It alerts the processor that some event has taken place.

But why are they called flags?

The possible solution is from the small flags which are found on the mail boxes in America. The small flag indicates that there is a mail in the mail box. Similarly this denotes that an event has occurred in the processor.

Intel processors have a set of 5 flags.

Carry flag

Parity flag

Auxiliary carry flag

Zero flag

Sign flag

Consider two binary numbers. For example:

1100 0000

1000 0000

When we add the above two numbers, a carry is generated in the most significant bit. The number in the extreme right is least significant bit, while the number in extreme left is most significant bit. So a ninth bit is generated due to the carry. So how to accommodate 9th bit in an 8 bit register? For this purpose the Carry flag is used. The carry flag is set whenever a carry is generated and reset whenever there is no carry. But there is an auxiliary carry flag? What is the difference between the carry flag and auxiliary carry flag?

Let's discuss with an example. Consider the two numbers given below 0000 0100, 0000 0101. When we add both the numbers a carry is generated in the third bit from the least significant bit. This sets the auxiliary carry flag. When there is no carry, the auxiliary carry flag is reset. So whenever there is a carry in the most significant bit Carry flag is set. While an auxiliary carry flag is set only when a carry is generated in bits other than the most significant bit. Parity checks whether it's even or odd parity. This flag returns a 0 if it is odd parity and returns a 1 if it is an even parity. Sometimes

they are also called as parity bit which is used to check errors while data transmission is carried out. Zero flag shows whether the output of the operation is 0 or not. If the value of Zero flag is 0 then the result of operation is not zero. If it is zero the flag returns value 1. Sign flag shows whether the output of operation has positive sign or negative sign. A value 0 is returned for positive sign and 1 is returned for negative sign.

Instruction Register and Decoder

Instruction register is 8-bit register just like every other register of microprocessor. Consider an instruction. The instruction may be anything like adding two data's, moving a data, copying a data etc. When such an instruction is fetched from memory, it is directed to Instruction register. So the instruction registers are specifically to store the instructions that are fetched from memory. There is an Instruction decoder which decodes the information present in the Instruction register for further processing.

Timing and Control Unit

Timing and control unit is a very important unit as it synchronizes the registers and flow of data through various registers and other units. This unit consists of an oscillator and controller sequencer which sends control signals needed for internal and external control of data and other units. The oscillator generates two-phase clock signals which aids in synchronizing all the registers of 8085 microprocessor.

Signals that are associated with Timing and control unit are:

Control Signals: READY, RD[⌚], WR[⌚], ALE

Status Signals: S0, S1, IO/M[⌚]

DMA Signals: HOLD, HLDA

RESET Signals: RESET IN, RESET OUT

Interrupt Control

As the name suggests this control interrupts a process. Consider that a microprocessor is executing the main program. Now whenever the interrupt signal is enabled or requested the microprocessor shifts the control from main program to process the incoming request and after the completion of request, the control goes back to the main program. For example an Input/output device may send an interrupt signal to notify that the data is ready for input. The microprocessor temporarily stops the execution of main program and transfers control to I/O device. After collecting the input data the control is transferred back to main program.

Interrupt signals present in 8085 are:

INTR

RST 7.5

RST 6.5

RST 5.5

TRAP

Of the above four interrupts TRAP is a NON-MASKABLE interrupt control and other three are **maskable** interrupts. A non-maskable interrupt is an interrupt which is given the highest priority in the order of interrupts. Suppose you want an instruction to be processed immediately, then you can give the instruction as a non-maskable interrupt. Further the non-maskable interrupt cannot be disabled by programmer at any point of time. Whereas the maskable interrupts can be disabled and enabled using EI and DI instructions. Among the maskable interrupts RST 7.5 is given the highest priority above RST 6.5 and least priority is given to INTR.

Serial I/O control

The input and output of serial data can be carried out using 2 instructions in 8085.

SID-Serial Input Data

SOD-Serial Output Data

Two more instructions are used to perform serial-parallel conversion needed for serial I/O devices. SIM

RIM

Address buffer and Address-Data buffer

The contents of the stack pointer and program counter are loaded into the address buffer and address-data buffer. These buffers are then used to drive the external address bus and address-data bus. As the memory and I/O chips are connected to these buses, the CPU can exchange desired data to the memory and I/O chips. The address-data buffer is not only connected to the external data bus but also to the internal data bus which consists of 8-bits. The address data buffer can both send and receive data from internal data bus.

Address bus and Data bus:

We know that 8085 is an 8-bit microprocessor. So the data bus present in the microprocessor is also 8-bits wide. So 8-bits of data can be transmitted from or to the microprocessor. But 8085 processor requires 16 bit address bus as the memory addresses are 16-bit wide. The 8 most significant bits of the address are transmitted with the help of address bus and the 8 least significant bits are transmitted with the

help of multiplexed address/data bus. The eight bit data bus is multiplexed with the eight least significant bits of address bus. The address/data bus is time multiplexed. This means for few microseconds, the 8 least significant bits of address are generated, while for next few seconds the same pin generates the data. This is called Time multiplexing. But there are situations where there is a need to transmit both data and address simultaneously. For this purpose a signal called ALE (address latch enable) is used. ALE signal holds the obtained address in its latch for a long time until the data is obtained and so when the microprocessor sends the data next time the address is also available at the output latch. This technique is called Address/Data demultiplexing.

2. With examples, explain the data transfer & arithmetic instructions of 8085. (AUC MAY 2012).

Instruction set of 8085 is classified as

- Data transfer or copy instructions
- Arithmetic instructions
- Logical instructions
- Branching instructions
- Machine Control instructions

DATA TRANSFER INSTRUCTIONS

Move 8 bit Register

MOV Rd, Rs: This instruction copies the contents of the source M, Rs register into the destination register; the contents of Rd, M the source register are not altered. If one of the operands is a memory location, its location is specified by the contents of the HL registers.

Example: MOV B, C or MOV B, M

Move immediate 8-bit

MVI Rd, data: The 8-bit data is stored in the destination register or M, data memory. If the operand is a memory location, its location is specified by the contents of the HL registers.

Example: MVI B, 57H or MVI M, 57H

Load accumulator

LDA 16-bit address: The contents of a memory location, specified by a 16-bit address in the operand, are copied to the accumulator. The contents of the source are not altered.

Example: LDA 2034H

Load accumulator indirect

LDAX B/D Reg. pair: The contents of the designated register pair point to a memory location. This instruction copies the contents of that memory location into the accumulator. The contents of either the register pair or the memory location are not altered.

Example: LDAX B

Load register pair immediate

LXI Reg. pair, 16-bit data: The instruction loads 16-bit data in the register pair designated in the operand.

Example: LXI H, 2034H or LXI H, XYZ

Load H and L registers direct

LHLD 16-bit address: The instruction copies the contents of the memory location pointed out by the 16-bit address into register L and copies the contents of the next memory location into register H. The contents of source memory locations are not altered.

Example: LHLD 2040H

Store accumulator direct

STA 16-bit address: The contents of the accumulator are copied into the memory location specified by the operand. This is a 3-byte instruction, the second byte specifies the low-order address and the third byte specifies the high-order address.

Example: STA 4350H

Store accumulator indirect

STAX Reg. pair: The contents of the accumulator are copied into the memory location specified by the contents of the operand (register pair). The contents of the accumulator are not altered.

Example: STAX B

Store H and L registers direct

SHLD 16-bit address: The contents of register L are stored into the memory location specified by the 16-bit address in the operand and the contents of H register are stored into the next memory location by incrementing the operand. The contents of

registers HL are not altered. This is a 3-byte instruction, the second byte specifies the low-order address and the third byte specifies the high-order address.

Example: SHLD 2470H

Exchange H and L with D and E

XCHG none: The contents of register H are exchanged with the contents of register D, and the contents of register L are exchanged with the contents of register E.

Example: XCHG

Copy H and L registers to the stack pointer

SPHL none: The instruction loads the contents of the H and L registers into the stack pointer register, the contents of the H register provide the high-order address and the contents of the L register provide the low-order address. The contents of the H and L registers are not altered.

Example: SPHL

Exchange H and L with top of stack

XTHL none: The contents of the L register are exchanged with the stack location pointed out by the contents of the stack pointer register. The contents of the H register are exchanged with the next stack location (SP+1); however, the contents of the stack pointer register are not altered.

Example: XTHL

Push register pair onto stack

PUSH Reg. pair: The contents of the register pair designated in the operand are copied onto the stack in the following sequence. The stack pointer register is decremented and the contents of the high order register (B, D, H, A) are copied into that location. The stack pointer register is decremented again and the contents of the low-order register (C, E, L, flags) are copied to that location.

Example: PUSH B or PUSH A

Pop off stack to register pair

POP Reg. pair: The contents of the memory location pointed out by the stack pointer register are copied to the low-order register (C, E, L, status flags) of the operand. The stack pointer is incremented by 1 and the contents of that memory location are copied to the high-order register (B, D, H, A) of the operand. The stack pointer register is again incremented by 1.

Example: POP H or POP A

Output data from accumulator to a port with 8-bit address

OUT 8-bit port address: The contents of the accumulator are copied into the I/O port specified by the operand.

Example: OUT F8H

IN 8-bit port address: Input data to accumulator from a port with 8-bit address. The contents of the input port designated in the operand are read and loaded into the accumulator.

Example: IN 8CH

ARITHMETIC INSTRUCTIONS

Add register or memory to accumulator

ADD R: The contents of the operand (register or memory) are added to the contents of the accumulator and the result is stored in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the addition.

Example: ADD B or ADD M

Add register to accumulator with carry

ADC R: The contents of the operand (register or memory) and the Carry flag are added to the contents of the accumulator and the result is stored in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the addition.

Example: ADC B or ADC M

Add immediate to accumulator

ADI 8-bit data: The 8-bit data (operand) is added to the contents of the accumulator and the result is stored in the accumulator. All flags are modified to reflect the result of the addition.

Example: ADI 45H

Add immediate to accumulator with carry

ACI 8-bit data: The 8-bit data (operand) and the Carry flag are added to the contents of the accumulator and the result is stored in the accumulator. All flags are modified to reflect the result of the addition.

Example: ACI 45H

Add register pair to H and L registers

DAD Reg. pair: The 16-bit contents of the specified register pair are added to the contents of the HL register and the sum is stored in the HL register. The contents of

the source register pair are not altered. If the result is larger than 16 bits, the CY flag is set. No other flags are affected.

Example: DAD H

Subtract register or memory from accumulator

SUB R: The contents of the operand (register or memory) are M subtracted from the contents of the accumulator, and the result is stored in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the subtraction.

Example: SUB B or SUB M

Subtract source and borrow from accumulator

SBB R: The contents of the operand (register or memory) and M the Borrow flag are subtracted from the contents of the accumulator and the result is placed in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the subtraction.

Example: SBB B or SBB M

Subtract immediate from accumulator

SUI 8-bit data: The 8-bit data (operand) is subtracted from the contents of the accumulator and the result is stored in the accumulator. All flags are modified to reflect the result of the subtraction.

Example: SUI 45H

Subtract immediate from accumulator with borrow

SBI 8-bit data: The 8-bit data (operand) and the Borrow flag are subtracted from the contents of the accumulator and the result is stored in the accumulator. All flags are modified to reflect the result of the subtraction.

Example: SBI 45H

Increment register or memory by 1

INR R: The contents of the designated register or memory) are M incremented by 1 and the result is stored in the same place. If the operand is a memory location, its location is specified by the contents of the HL registers.

Example: INR B or INR M

Increment register pair by 1

INX R: The contents of the designated register pair are incremented by 1 and the result is stored in the same place.

Example: INX H

Decrement register or memory by 1

DCR R: The contents of the designated register or memory are M decremented by 1 and the result is stored in the same place. If the operand is a memory location, its location is specified by the contents of the HL registers.

Example: DCR B or DCR M

Decrement register pair by 1

DCX R: The contents of the designated register pair are decremented by 1 and the result is stored in the same place.

Example: DCX H

Decimal adjust accumulator

DAA none : The contents of the accumulator are changed from a binary value to two 4-bit binary coded decimal (BCD) digits. This is the only instruction that uses the auxiliary flag to perform the binary to BCD conversion, and the conversion procedure is described below. S, Z, AC, P, CY flags are altered to reflect the results of the operation. If the value of the low-order 4-bits in the accumulator is greater than 9 or if AC flag is set, the instruction adds 6 to the low-order four bits. If the value of the high-order 4-bits in the accumulator is greater than 9 or if the Carry flag is set, the instruction adds 6 to the high-order four bits.

Example: DAA

BRANCHING INSTRUCTIONS

Jump unconditionally

JMP 16-bit address: The program sequence is transferred to the memory location specified by the 16-bit address given in the operand.

Example: JMP 2034H or JMP XYZ

Jump conditionally Operand 16-bit address:

The program sequence is transferred to the memory location specified by the 16-bit address given in the operand based on the specified flag of the PSW as described below.

Example: JZ 2034H or JZ XYZ

Opcode Description Flag Status

JC Jump on Carry CY = 1

JNC Jump on no Carry CY = 0

JP Jump on positive S = 0

JM Jump on minus S = 1

JZ Jump on zero Z = 1

JNZ Jump on no zero Z = 0

JPE Jump on parity even P = 1

JPO Jump on parity odd P = 0

Unconditional subroutine call

CALL 16-bit address: The program sequence is transferred to the memory location specified by the 16-bit address given in the operand. Before the transfer, the address of the next instruction after CALL (the contents of the program counter) is pushed onto the stack.

Example: CALL 2034H or CALL XYZ

Call conditionally Operand 16-bit address

The program sequence is transferred to the memory location specified by the 16-bit address given in the operand based on the specified flag of the PSW as described below. Before the transfer, the address of the next instruction after the call (the contents of the program counter) is pushed onto the stack.

Example: CZ 2034H or CZ XYZ

Opcode Description Flag Status

CC Call on Carry CY = 1

CNC Call on no Carry CY = 0

CP Call on positive S = 0

CM Call on minus S = 1

CZ Call on zero Z = 1

CNZ Call on no zero Z = 0

CPE Call on parity even P = 1

CPO Call on parity odd P = 0

field flag of the PSW as described below. The two bytes from the top of the stack are copied into the program counter, and program execution begins at the new address.

Example: RZ

Opcode Description Flag Status

RC Return on Carry CY = 1

RNC Return on no Carry CY = 0

RP Return on positive S = 0

RM Return on minus S = 1

RZ Return on zero Z = 1

RNZ Return on no zero Z = 0

RPE Return on parity even $P = 1$

RPO Return on parity odd $P = 0$

Load program counter with HL contents

PCHL none: The contents of registers H and L are copied into the program counter. The contents of H are placed as the high-order byte and the contents of L as the low-order byte.

Example: PCHL

Restart

RST 0-7: The RST instruction is equivalent to a 1-byte call instruction to one of eight memory locations depending upon the number. The instructions are generally used in conjunction with interrupts and inserted using external hardware. However these can be used as software instructions in a program to transfer program execution to one of the eight locations. The addresses are:

Instruction Restart Address

RST 0 0000H

RST 1 0008H

RST 2 0010H

RST 3 0018H

RST 4 0020H

RST 5 0028H

RST 6 0030H

RST 7 0038H

The 8085 has four additional interrupts and these interrupts generate RST instructions internally and thus do not require any external hardware. These instructions and their Restart addresses are:

Interrupt Restart Address TRAP 0024H

RST 5.5 002CH

RST 6.5 0034H

RST 7.5 003CH

LOGICAL INSTRUCTIONS

Compare register or memory with accumulator

CMP R: The contents of the operand (register or memory) are M compared with the contents of the accumulator. Both contents are preserved. The result of the comparison is shown by setting the flags of the PSW as follows:

if $(A) < (\text{reg/mem})$: carry flag is set if $(A) = (\text{reg/mem})$: zero flag is set

if (A) > (reg/mem): carry and zero flags are reset

Example: CMP B or CMP M

Compare immediate with accumulator

CPI 8-bit data: The second byte (8-bit data) is compared with the contents of the accumulator. The values being compared remain unchanged. The result of the comparison is shown by setting

the flags of the PSW as follows: if (A) < data: carry flag is set

if (A) = data: zero flag is set

if (A) > data: carry and zero flags are reset

Example: CPI 89H

Logical AND register or memory with accumulator

ANA R: The contents of the accumulator are logically ANDed with M the contents of the operand (register or memory), and the result is placed in the accumulator. If the operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY is reset. AC is set.

Example: ANA B or ANA M

Logical AND immediate with accumulator

ANI 8-bit data :The contents of the accumulator are logically ANDed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY is reset. AC is set.

Example: ANI 86H

Exclusive OR register or memory with accumulator

XRA R: The contents of the accumulator are Exclusive ORed with M the contents of the operand (register or memory), and the result is placed in the accumulator. If the operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.

Example: XRA B or XRA M

Exclusive OR immediate with accumulator

XRI 8-bit data: The contents of the accumulator are Exclusive ORed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.

Example: XRI 86H

Logical OR register or memory with accumulator

ORA R:The contents of the accumulator are logically ORed with M the contents of the operand (register or memory), and the result is placed in the accumulator. If the

operand is a memory location, its address is specified by the contents of HL registers. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.

Example: ORA B or ORA M

Logical OR immediate with accumulator

ORI 8-bit data The contents of the accumulator are logically ORed with the 8-bit data (operand) and the result is placed in the accumulator. S, Z, P are modified to reflect the result of the operation. CY and AC are reset.

Example: ORI 86H

Rotate accumulator left

RLC none: Each binary bit of the accumulator is rotated left by one position. Bit D7 is placed in the position of D0 as well as in the Carry flag. CY is modified according to bit D7. S, Z, P, AC are not affected.

Example: RLC

Rotate accumulator right

RRC none: Each binary bit of the accumulator is rotated right by one position. Bit D0 is placed in the position of D7 as well as in the Carry flag. CY is modified according to bit D0. S, Z, P, AC are not affected.

Example: RRC

Rotate accumulator left through carry

RAL none: Each binary bit of the accumulator is rotated left by one position through the Carry flag. Bit D7 is placed in the Carry flag, and the Carry flag is placed in the least significant position D0. CY is modified according to bit D7. S, Z, P, AC are not affected.

Example: RAL

Rotate accumulator right through carry

RAR none: Each binary bit of the accumulator is rotated right by one position through the Carry flag. Bit D0 is placed in the Carry flag, and the Carry flag is placed in the most significant position D7. CY is modified according to bit D0. S, Z, P, AC are not affected.

Example: RAR

Complement accumulator

CMA none: The contents of the accumulator are complemented. No flags are affected.

Example: CMA

Complement carry

CMC none: The Carry flag is complemented. No other flags are affected.

Example: CMC

Set Carry

STC none: The Carry flag is set to 1. No other flags are affected.

Example: STC

CONTROL INSTRUCTIONS

No operation

NOP none: No operation is performed. The instruction is fetched and decoded. However no operation is executed.

Example: NOP

Halt and enter wait state

HLT none: The CPU finishes executing the current instruction and halts any further execution. An interrupt or reset is necessary to exit from the halt state.

Example: HLT

Disable interrupts

DI none: The interrupt enable flip-flop is reset and all the interrupts except the TRAP are disabled. No flags are affected.

Example: DI

Enable interrupts

EI none: The interrupt enable flip-flop is set and all interrupts are enabled. No flags are affected. After a system reset or the acknowledgement of an interrupt, the interrupt enable flipflop is reset, thus disabling the interrupts. This instruction is necessary to reenable the interrupts (except TRAP).

Example: EI

3. What are the addressing modes supported in 8085 CPU? Explain each of them with minimum of 2 sample instructions. (AUC MAY 2010)

ADDRESSING MODES

Every instruction of a program has to operate on a data. The method of specifying the data to be operated by the instruction is called Addressing. The 8085 has the following 5 different types of addressing.

1. Immediate Addressing
2. Direct Addressing
3. Register Addressing
4. Register Indirect Addressing
5. Implied Addressing

1. **Immediate Addressing:**

In immediate addressing mode, the data is specified in the instruction itself. The data will be a part of the program instruction.

EX. MVI B, 3EH - Move the data 3EH given in the instruction to B register; LXI SP, 2700H.

2. Direct Addressing:

In direct addressing mode, the address of the data is specified in the instruction.

The data will be in memory. In this addressing mode, the program instructions and data can be stored in different memory.

EX. LDA 1050H - Load the data available in memory location 1050H in to accumulator; SHLD 3000H

3. Register Addressing:

In register addressing mode, the instruction specifies the name of the register in which the data is available.

EX. MOV A, B - Move the content of B register to A register; SPHL; ADD C.

4. Register Indirect Addressing:

In register indirect addressing mode, the instruction specifies the name of the register in which the address of the data is available. Here the data will be in memory and the address will be in the register pair.

EX. MOV A, M - The memory data addressed by H L pair is moved to A register.
LDAX B.

5. Implied Addressing:

In implied addressing mode, the instruction itself specifies the data to be operated.

EX. CMA - Complement the content of accumulator; RAL

4. The following block of data is stored in the memory location from 4000H to 4005H. transfer the data to the location 5000H to 5005H in the reverse order. Write an ALP in 8085 to perform block transfer. 22H, A5H, B2H, 99H, 7FH, 37H. (AUC MAY 2011)

Algorithm

- 1) Load the DE pair with the destination address.
- 2) Load the HL pair with the count of elements in the data block.
- 3) Load element in the data block.
- 4) Increment the source address.
- 5) Copy the element to the accumulator and then transfer it to the destination address.
- 6) Increment destination address.
- 7) Decrement the count.
- 8) If Count = 0 then go to the next step else go to step 3.
- 9) Terminate the program.

MEMORY	LABEL	MNEMONIC	OPCODE	COMMENT
4200		LXI D,5000	11	Load destination address in DE pair
4201			00	
4202			45	
4203		LXI H,4000	21	Load the count in HL pair
4204			00	
4205			41	
4206		MOV C,M	4E	Copy the count to register C
4207	LOOP	INX H	23	Increment memory
4208		MOV A,M	7E	Copy element to Accumulator
4209		STAX D	12	Store the element to the address in the DE pair
420A		INX D	13	Increment destination address
420B		DCR C	OD	Decrement count
420C		JNZ LOOP	C2	Jump on non-zero to the label LOOP
420D			07	
420E			42	
420F		HLT	76	Program ends

Observation

Input at	4000	:	22 _H
	4001	:	A5 _H
	4002	:	B2 _H
	4003	:	99 _H
	4004	:	7F _H
	4005	:	37 _H
Output at	5000	:	22 _H
	5001	:	A5 _H
	5002	:	B2 _H
	5003	:	99 _H
	5004	:	7F _H
	5005	:	37 _H

5. Explain the interrupt structure of 8085 CPU with the required diagrams. (AUC MAY 2011)

Interrupt Structure in 8085

- Interrupt is signals send by an external device to the processor, to request the processor to perform a particular task or work.
- Mainly in the microprocessor based system the interrupts are used for data transfer between the peripheral and the microprocessor.
- The processor will check the interrupts always at the 2nd T-state of last machine cycle.
- If there is any interrupt it accept the interrupt and send the INTA (active low) signal to the peripheral.
- The vectored address of particular interrupt is stored in program counter.
- The processor executes an interrupt service routine (ISR) addressed in program counter.
- It returned to main program by RET instruction.

Types of Interrupts:

It supports two types of interrupts.

- **Hardware**
- **Software**

Software interrupts:

- The software interrupts are program instructions. These instructions are inserted at desired locations in a program.
- The 8085 has eight software interrupts from RST 0 to RST 7. The vector address for these interrupts can be calculated as follows.
- Interrupt number * 8 = vector address
- For RST 5, $5 * 8 = 40 = 28H$
- Vector address for interrupt RST 5 is 0028H

The Table shows the vector addresses of all interrupts.

Interrupt	Vector address
RST 0	0000 _H
RST 1	0008 _H
RST 2	0010 _H
RST 3	0018 _H
RST 4	0020 _H
RST 5	0028 _H
RST 6	0030 _H
RST 7	0038 _H

Hardware interrupts:

- An external device initiates the hardware interrupts and placing an appropriate signal at the interrupt pin of the processor.
- If the interrupt is accepted then the processor executes an interrupt service routine.

The 8085 has five hardware interrupts

(1) TRAP (2) RST 7.5 (3) RST 6.5 (4) RST 5.5 (5) INTR

Interrupt	Vector address
RST 7.5	003C _H
RST 6.5	0034 _H
RST 5.5	002C _H
TRAP	0024 _H

TRAP:

- This interrupt is a non-maskable interrupt. It is unaffected by any mask or interrupt enable.
- TRAP has the highest priority and vectored interrupt.
- TRAP interrupt is edge and level triggered. This means that the TRAP must go high and remain high until it is acknowledged.
- In sudden power failure, it executes a ISR and send the data from main memory to backup memory.
- The signal, which overrides the TRAP, is HOLD signal. (i.e., If the processor receives HOLD and TRAP at the same time then HOLD is recognized first and then TRAP is recognized).
- **There are two ways to clear TRAP interrupt.**

1.By resetting microprocessor (External signal)

2.By giving a high TRAP ACKNOWLEDGE (Internal signal)

RST 7.5:

The RST 7.5 interrupt is a maskable interrupt.

- It has the second highest priority.
- It is edge sensitive. ie. Input goes to high and no need to maintain high state until it recognized.
- Maskable interrupt. It is disabled by,
 - 1.DI instruction
 - 2.System or processor reset.
 - 3.After reorganization of interrupt.
- Enabled by EI instruction.

RST 6.5 and 5.5:

- The RST 6.5 and RST 5.5 both are level triggered. . ie. Input goes to high and stay high until it recognized.
- Maskable interrupt. It is disabled by,
 - 1.DI, SIM instruction
 - 2.System or processor reset.
 - 3.After reorganization of interrupt.
- Enabled by EI instruction.
- The RST 6.5 has the third priority whereas RST 5.5 has the fourth priority.

INTR:

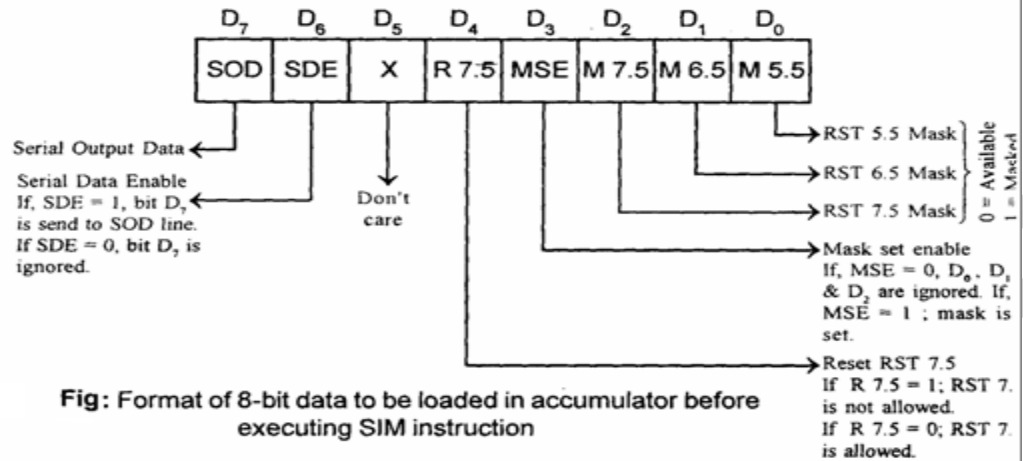
- INTR is a maskable interrupt. It is disabled by,

1. DI, SIM instruction
2. System or processor reset.
3. After reorganization of interrupt.

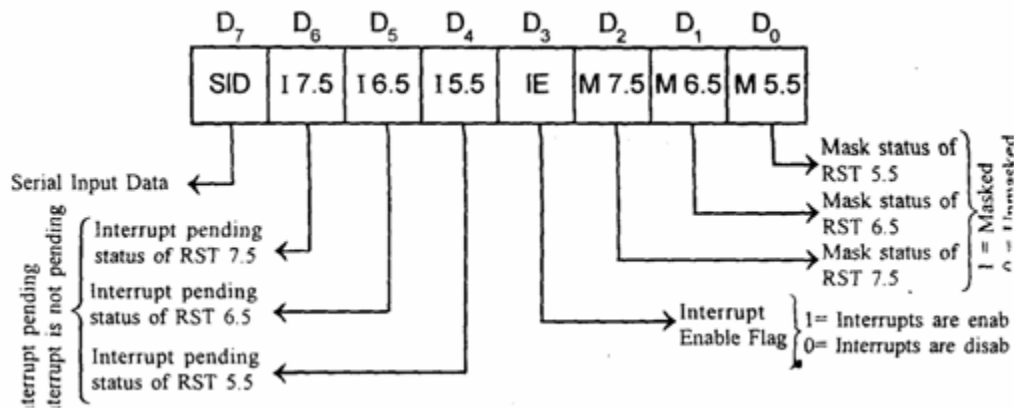
- Enabled by EI instruction.
- Non- vectored interrupt. After receiving INTA (active low) signal, it has to supply the address of ISR.
- It has lowest priority.
- It is a level sensitive interrupts. i.e. Input goes to high and it is necessary to maintain high state until it recognized.
- **The following sequence of events occurs when INTR signal goes high.**
 - 1. The 8085 checks the status of INTR signal during execution of each instruction.
 - 2. If INTR signal is high, then 8085 complete its current instruction and sends active low interrupt acknowledge signal, if the interrupt is enabled.
 - 3. In response to the acknowledge signal, external logic places an instruction OPCODE on the data bus. In the case of multibyte instruction, additional interrupt acknowledge machine cycles are generated by the 8085 to transfer the additional bytes into the microprocessor.
 - 4. On receiving the instruction, the 8085 save the address of next instruction on stack and execute received instruction.

SIM and RIM for interrupts:

- The 8085 provide additional masking facility for RST 7.5, RST 6.5 and RST 5.5 using SIM instruction.
- The status of these interrupts can be read by executing RIM instruction.
- The masking or unmasking of RST 7.5, RST 6.5 and RST 5.5 interrupts can be performed by moving an 8-bit data to accumulator and then executing SIM instruction.
- The format of the 8-bit data is shown below.



- The status of pending interrupts can be read from accumulator after executing RIM instruction.
- When RIM instruction is executed an 8-bit data is loaded in accumulator, which can be interpreted as shown in fig.



Interrupt type	Trigger	Priority	Maskable	Vector address
TRAP	Edge and Level	1 st	No	0024H
RST 7.5	Edge	2 nd	Yes	003CH
RST 6.5	Level	3 rd	Yes	0034H
RST 5.5	Level	4 th	Yes	002CH
INTR	Level	5 th	Yes	-

- Write a simple program to sort the given numbers in ascending & descending order.(AUC NOV 2010)

Program to sort the numbers in ascending order

Explanation :

- Consider that a block of N words is present. Now we have to arrange these N words in ascending order, Let N = 4 for example. We will use HL as pointer to point the block of N words.
- Initially in the first iteration we compare first number with the second number. If first number < second number, don't interchange the contents, otherwise if first number > second number swap the contents.
- In the next iteration we go on comparing the first number with third number. If first number < third number, don't interchange the contents. If first number > third number then swapping will be done.
- Since the first two numbers are in ascending order the third number will go to first place, first number in second place and second number will come in third place in the second iteration only if first number > third number.
- In the next iteration first number is compared with fourth number. So comparisons are done till all N numbers are arranged in ascending order. This method requires approximately n comparisons.

Algorithm

- Step I : Initialize the number of elements counter.
- Step II : Initialize the number of comparisons counter.
- Step III : Compare the elements. If first element < second element goto step VIII else goto step V for(ASC). If first element > second element goto step VIII else goto step V for (DES)
- Step IV : Swap the elements.
- Step V : Decrement the comparison counter.
- Step VI : Is count = 0 ? if yes goto step VIII else goto step IV.
- Step VII : Insert the number in proper position
- Step VIII : Increment the number of elements counter.
- Step IX : Is count = N ? If yes, goto step XI else goto step II
- Step X : Store the result.
- Step XI : Stop.

Ascending order Program:

Instruction	Comment
MVI B, 09	; Initialize counter 1
START: LXI H, D000H	; Initialize memory pointer
MVI C, 09H	; Initialize counter 2
BACK: MOV A, M	; Get the number in accumulator
INX H	; Increment memory pointer
CMP M	; Compare number with next number
JC SKIP	; If less, don't interchange
JZ SKIP	; If equal, don't interchange
MOV D, M	; Otherwise swap the contents
MOV M, A	
DCX H	; Interchange numbers
MOV M, D	
INX H	; Increment pointer to next memory location
SKIP: DCR C	; Decrement counter 2
JNZ BACK	; If not zero, repeat
DCR B	; Decrement counter 1
JNZ START	; If not zero, repeat
HLT	; Terminate program
execution	

Descending order Program:

Instruction	Comment
MVI B, 09	; Initialize counter 1
START: LXI H, D000H	; Initialize memory pointer
MVI C, 09H	; Initialize counter 2
BACK: MOV A, M	; Get the number in accumulator


```
        INX    H                ; Increment memory pointer
        CMP    M                ; Compare number with next
number
        JNC    SKIP            ; If less, don't interchange
        JZ     SKIP            ; If equal, don't interchange
        MOV    D, M            ; Otherwise swap the contents
        MOV    M, A
        DCX    H                ; Interchange numbers
        MOV    M, D
        INX    H                ; Increment pointer to next
memory location
SKIP:    DCR    C                ; Decrement counter 2
        JNZ    BACK            ; If not zero, repeat
        DCR    B                ; Decrement counter 1
        JNZ    START           ; If not zero, repeat
        HLT                     ; Terminate program
execution
```

7. Explain the classification of instruction set of the microprocessor 8085. (AUC NOV 2011)

Same as Q2

QUESTION BANK

DEPARTMENT: ME

YR/ SEM:II/ III

SUB CODE: ME2255

**SUB NAME: ELECTRONICS
& MICROPROCESSORS**

UNIT 5- INTERFACING & APPLICATIONS OF MICROPROCESSOR

PART A (2 Marks)

1. What do you mean by interfacing? (AUC MAY 2012)

Interfacing is connection external I/O devices to the microprocessor for various applications. To communicate with the outside world microprocessors use peripherals (I/O devices). The connection circuits are called interfacing circuits.

2. List out some applications of microprocessor. (AUC MAY 2012, NOV 2011)

- To measure & control the temperature
- To control the speed of motors.
- To control the traffic light system
- To change the direction of motor rotation

3. Define interfacing devices. (AUC MAY 2010)

Interfacing devices are devices used to connect the peripherals to the processor. For example Programmable Peripheral Interface or Parallel communication chip (8255), Keyboard & Display controller (8279), Programmable Interrupt Controller (8259), USART(8251), Timer controller (8253).

4. What is transceiver? (AUC MAY 2010)

The device used for transmission & reception of data is called a transceiver. The transmitter & receiver is present in the same module.

5. What is the role of tristate buffer in interfacing of peripherals with CPU? (AUC MAY 2011)

It is a buffer which has one input line, one output line and an enable line. When the enable line is low the circuit acts as a buffer. When the enable line is high the circuit is in high impedance state.

6. Write the use of ALE signal in 8085. (AUC MAY 2011)
ALE, Address Latch Enable signal specifies whether the multiplexed bus is address or data bus.
7. List the fundamentals of I/O technique. (AUC NOV 2010)
Memory mapped I/O & I/O mapped I/O
8. List any two points comparing memory I/O and peripheral I/O. (AUC NOV 2010)

S.NO	Memory mapped I/O	I/O mapped I/O
1	I/O device is treated as memory location	I/O devices have separate address
2	The processor uses 16 bit address to identify an I/O device	The processor uses 8 bit address to identify an I/O device
3	Memory map is shared between memory & I/O device	256 I/O devices can be connected to the microprocessor

9. Define the term step angle with reference to a stepper motor. (AUC NOV 2011)
For a motor with 4 stator poles & 3 pairs of rotor poles (six) there are 12 possible stable positions in which a south pole of the rotor can lock with a north pole of the stator. The step size can be calculated from
Step size = $(360^\circ)/(N_s \cdot N_r)$
 N_s – is the number of stator poles
 N_r – is the number of rotor poles
For example $N_s=4$ & $N_r=3$
Step size = $(360^\circ)/(4 \cdot 3) = 30^\circ$

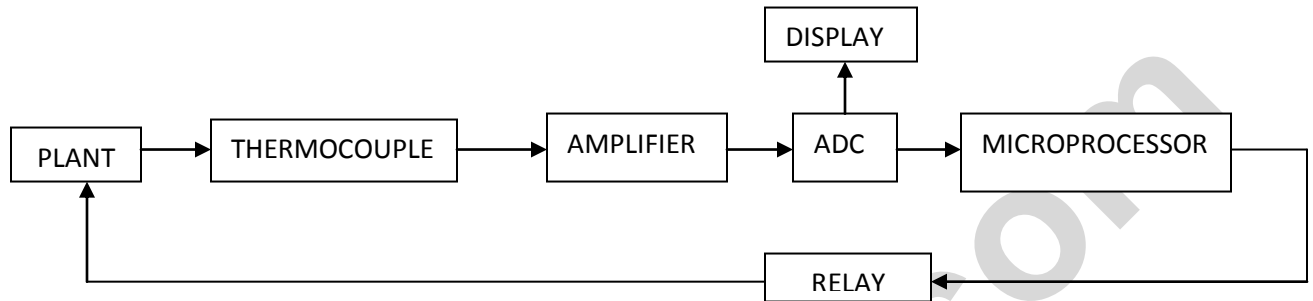
PART B (8,16 Marks)

1. Draw & explain the block diagram & operation of temperature controlling system with a microprocessor. (AUC MAY 2012, NOV 2010)

Temperature Control using 8085:

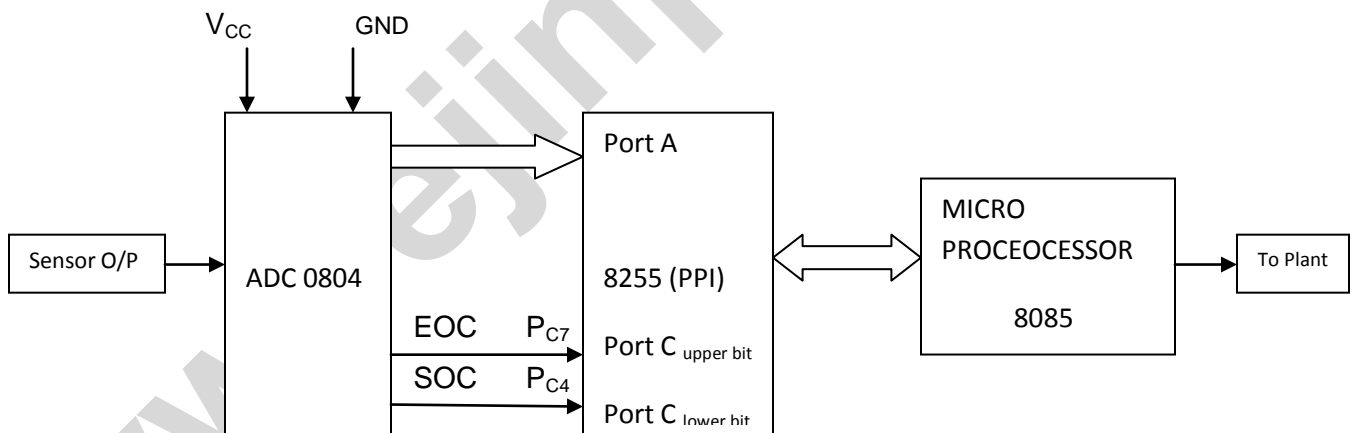
Microprocessor based systems are widely used in industries for the measurement, display & monitoring of physical quantities like temperature, pressure, speed.... For the measurements of physical quantities transducers are used to convert them to electrical quantities. The electrical output of the transducer is proportional to the

input quantity which may be temperature or some other physical quantity. If the electrical signal strength is low, then it is amplified using amplifiers. This electrical signal is applied to A/D converter which is connected to the microprocessor.



BLOCK DIAGRAM OF MICROPROCESSOR BASED TEMPERATURE CONTROL SYSTEM

For interfacing temperature control system with microprocessor, 8255(PPI) & suitable ADC are connected between microprocessor & sensor output. The below diagram shows the successive approximation A/D converter to the microprocessor unit through 8255



The microprocessor sends a start of conversion SOC signal to the A/D converter through the Port C lower of 8255. When A/D converter completes conversion, it sends as end of conversion EOC signal to the microprocessor. Having received an EOC signal from A/D converter, the microprocessor reads the output of the A/D converter which is a digital quantity of the temperature to be measured. The microprocessor displays the measured temperature. For control of temperature, the microprocessor compares the measured temperature with the reference value

& sends the control signal to reduce or increase the temperature based on desired temperature.. in this way the temperature is maintained.

ALGORITHM:

Step1: Initialize 8255 port A as input port, port C upper as an input port & port C lower as an output port.

Step2: Send SOC to A/D converter CL port.

Step3: Check for EOC from A/D converter, CU port

Step4: read the data from A/D converter.

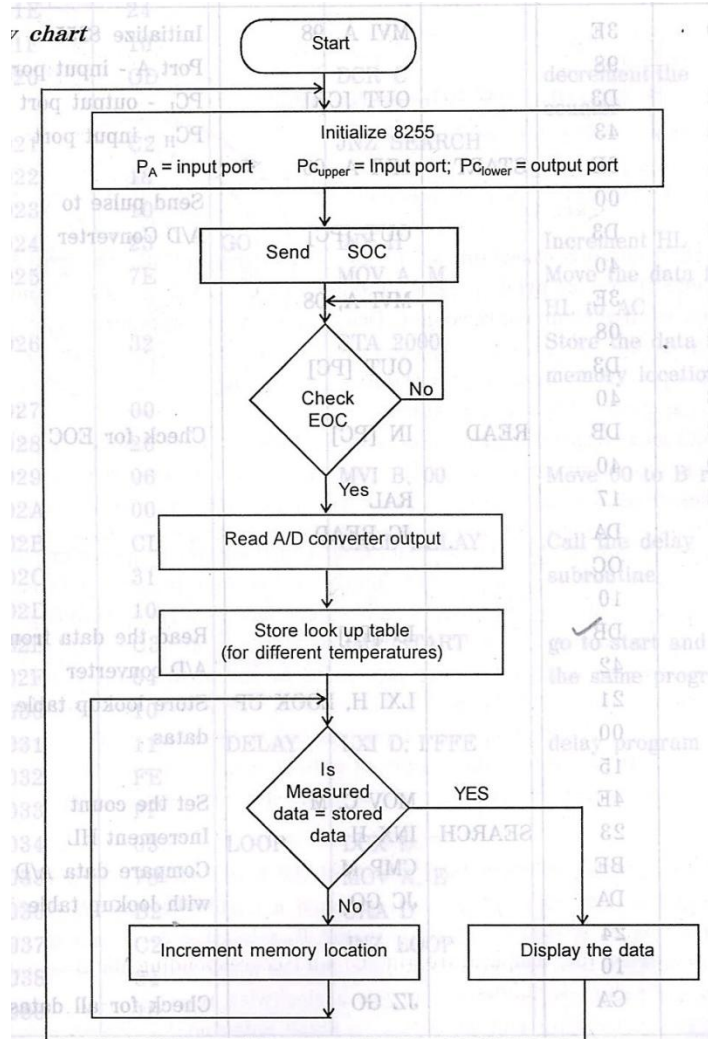
Step5: store the temperature in degrees & corresponding digital voltage in memory locations.

Step6: Compare the output of A/D converter with value in the memory location.

Step7: Display the equivalent value in degrees.

Step8: Repeat steps 2 to 7 for continuous temperature measurement & control.

FLOW CHART:



PROGRAM:

```

MVI A, 98
OUT[CR]
START MVI A, 00
OUT [PC]
MVI A, 08
OUT PC
READ IN [PC]
RAL
JC READ
IN [PA]
LXI H, LOOK UP
  
```

```
        MOV C,M
SEARCH INX H
        CMP M
        JC GO
        JZ GO
        DCR C
        JNZ SEARCH
        GO INX H
        MOV A,M
        STA 2000
        MVI B, 00
        CALL DELAY
        JMP START
DELAY LXI D, FFFE
LOOP  DCXD
      MOV A,E
      ORA D
      JNZ LOOP
```

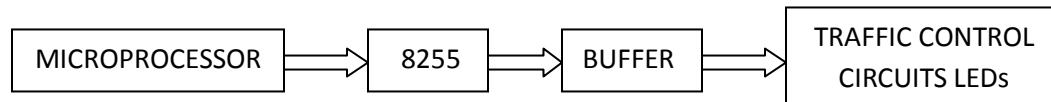
2. Draw & explain the block diagram & operation of traffic light controller with a microprocessor. (AUC MAY 2012, MAY 2010, MAY 2011, NOV 2010, NOV 2011)

Traffic Light Controller:

The signal lamps are controlled on the junction road by interfacing it with a microprocessor & the traffic sequence is controlled using it. A typical road junction is shown in figure, which is used as a model. Four identical sets of loght at each corner are provided. The marking on the set of lights at each corner means the following:

- RED – Stop crossing
- YELLOW - provides caution that traffic is about to stop or about to start
- GREEN – allows crossing

The below figure shows the block diagram of interfacing traffic light signal lamps with the microprocessor. Here all the ports of 8255 have been programmed as output ports. The control word to make all ports for MODE 0 operation is 80H.



The output of the 8255 ports is connected to the LEDs through buffers. Either positive logic or negative logic has been used to switch ON LEDs. Three types of LEDs are used as mentioned above such as RED, YELLOW, GREEN. The arrangement of traffic lights with 8255 ports is given below.

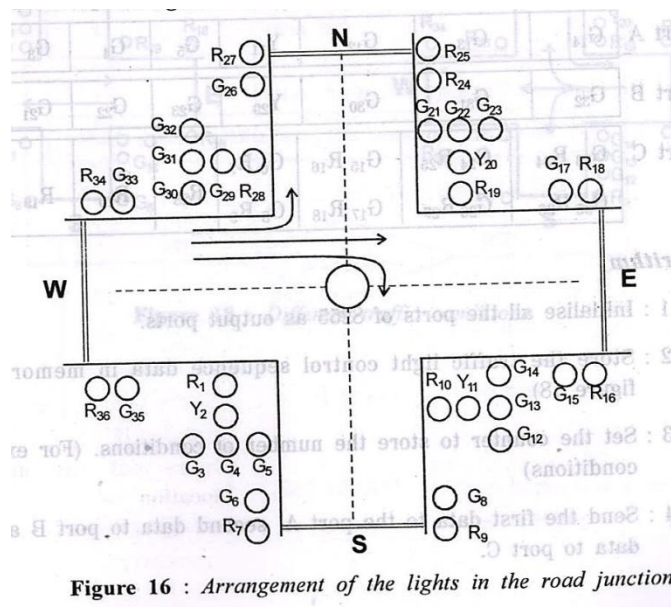


Figure 16 : Arrangement of the lights in the road junction

	PA ₇	PA ₆	PA ₅	PA ₄	PA ₃	PA ₂	PA ₁	PA ₀
PORT A	G ₁₄	G ₁₃	G ₁₂	Y ₁₁	G ₅	G ₄	G ₃	Y ₂
PORT B	G ₃₂	G ₃₁	G ₁₄	Y ₂₀	G ₂₃	G ₂₂	G ₂₁	Y ₂₀
PORT C	G ₃₃ R ₃₄	G ₂₄ R ₂₅	G ₁₅ R ₁₆	G ₆ R ₇	R ₂₈	R ₁₀	R ₁₉	R ₁
	G ₃₅ R ₃₆	G ₂₆ R ₂₇	G ₁₇ R ₁₈	G ₈ R ₉				

Algorithm:

Step1: initialize all the ports of 8255 as out ports.

Step2: store the traffic light control sequence data in memory

Step3: set the counter to store the number of conditions.

Step4: send the first data to the port A, second data to port B and third data to port C.

Step5: Call the subroutine for delay.

Step6: repeat the step 2 to step 6 for continuous control of lights in the road junction.

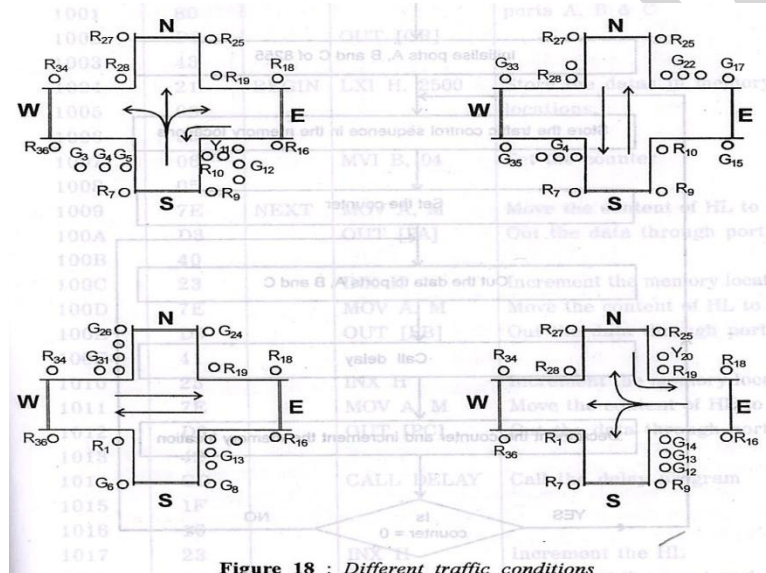
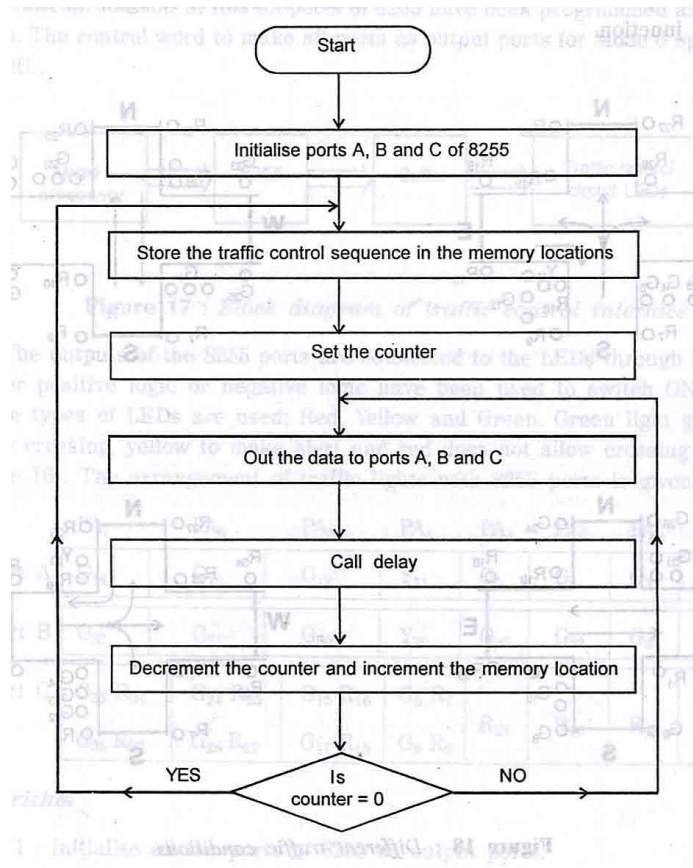


Figure 18 : Different traffic conditions

Flow Chart:



Program:

```

MVI A, 80
OUT [CR]
BEGIN LXI H, 2500
MVI B, 04
NEXT MOV A, M
OUT [PA]
INX H
MOV A, M
OUT [PB]
INX H
MOV A, M
  
```

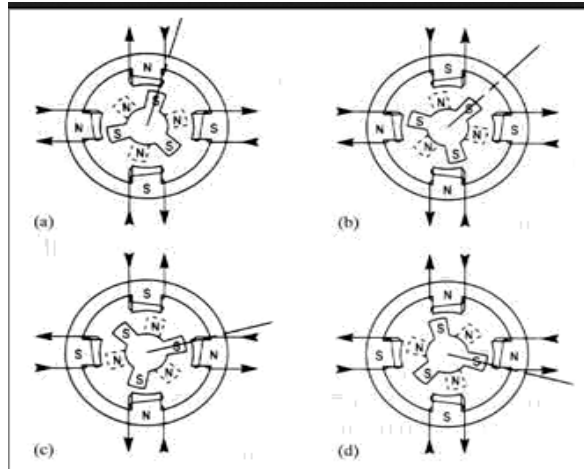
```
OUT [PC]
CALL DELAY
INX H
DCR B
JNZ NEXT
JMP BEGIN
DELAY LXI D, FFFF
LOOP DCX D
MOV A, E
ORA D
JNZ LOOP
RET
```

2500	3E	00	FE	Data1
2503	04	04	5C	Data2
2506	40	40	A3	Data3
2509	E0	01	F3	Data4

3. How to control the speed of stepper motor with 8085 CPU & its interface? Draw a neat diagram & explain its operation. (AUC MAY 2010, MAY 2011)

Stepper motor control:

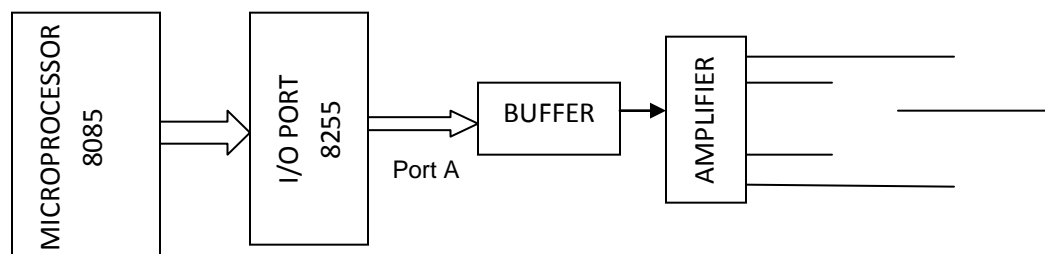
A stepper motor rotates in steps to digital pulse input. The shaft of the motor rotates in equal increments when a train of pulse is applied. To control the direction & number of steps appropriate pulses are applied to the stator winding of the motor. There are two common types of stepper motor one is permanent magnet type & the other is variable reluctance type. The below figure shows the permanent magnet type stepper motor with 4 pole stator & rotor with six permanent poles.



The stator is made of laminated soft iron. The stator windings are energized by pulses. The motor shown in figure has four phase excitation as there are four poles on the stator. Each pole has two coils wound in the opposite sense so that the pole can be made either a north pole or south pole as desired by applying appropriate pulse to one of the coils. If the pole A1 is made North Pole, the pole A2 is made South Pole. The permanent south pole no: 1 of the rotor will stand just below the pole A1 of the stator. To give clockwise motion, the supply of pole A1 & A2 is switched off and B1 & B2 are energized. The pole B1 is made a South Pole and B2 a north pole.

Now the permanent north pole no: 2 of the rotor comes just below the pole B1. In the next step the pole A2 is made a North Pole and A1 a south pole. After this B2 is made a south pole & B1 is a north pole. Again the pole A1 is made a north pole & A2 a south pole & the whole sequence is repeated. In this order poles are energized to give a clockwise rotation. To rotate the rotor anticlockwise after making A1 pole a north pole & A2 a south pole, B2 is made a south pole & B1 a north pole.

Block Diagram of Stepper Motor Interfacing with 8085.



The 12V DC supply is used to energize the poles. Pulses sent by the microprocessor switch on rated voltage to the windings of the desired pole. A delay subroutine is incorporated in the program. After energizing on set of pole windings some delay is provided, then the power supply is switched on to the other set of pole windings. This delay governs the speed of the motor.

For a motor with 4 stator poles & 3 pairs of rotor poles (six) there are 12 possible stable positions in which a south pole of the rotor can lock with a north pole of the stator. The step size can be calculated from

$$\text{Step size} = (360^\circ) / (N_s \cdot N_r)$$

N_s – is the number of stator poles

N_r – is the number of rotor poles

For example $N_s=4$ & $N_r=3$

$$\text{Step size} = (360^\circ) / (4 \cdot 3) = 30^\circ$$

Generally there are 3 different schemes available for stepping a stepper motor. They are,

- Wave scheme (unipolar operation)
- Two phase scheme
- Half stepping scheme

Wave Scheme:

In this, the stepper motor windings A_1 , B_1 , A_2 , B_2 are cyclically excited with a DC current to turn the motor in the clockwise direction. By reversing the phase sequence as A_1 , B_2 , A_2 , B_1 the motor can be made to run in the anti clockwise direction.

Table 3: Wave switching scheme

Anti clockwise						Clockwise					
Step	A_1	A_2	B_1	B_2		Step	A_1	A_2	B_1	B_2	
1	1	0	0	0	(80)	1	1	0	0	0	(80)
2	0	0	0	1	(01)	2	0	0	1	0	(02)
3	0	1	0	0	(04)	3	0	1	0	0	(04)
4	0	0	1	0	(02)	4	0	0	0	1	(01)

Two Phase scheme:

In this scheme any two adjacent windings are energized. The switching scheme for the operation is given in table 4.

Table 4: Two-phase switching scheme

Anti clockwise						Clockwise					
Step	A ₁	A ₂	B ₁	B ₂		Step	A ₁	A ₂	B ₁	B ₂	
1	1	0	0	1	(09)	1	1	0	1	0	(0A)
2	0	1	0	1	(05)	2	0	1	1	0	(06)
3	0	1	1	0	(06)	3	0	1	0	1	(05)
4	1	0	1	0	(0A)	4	1	0	0	1	(09)

Half stepping scheme:

The half stepping scheme is a mixture of the wave scheme & the 2 phase scheme & this increases the accuracy of the stepper motor. The switching sequence for half stepping scheme is given in table 5.

To interface a stepper motor with 8085 microprocessor, a set of instructions have to be executed. The algorithm, flowchart & program is given below.

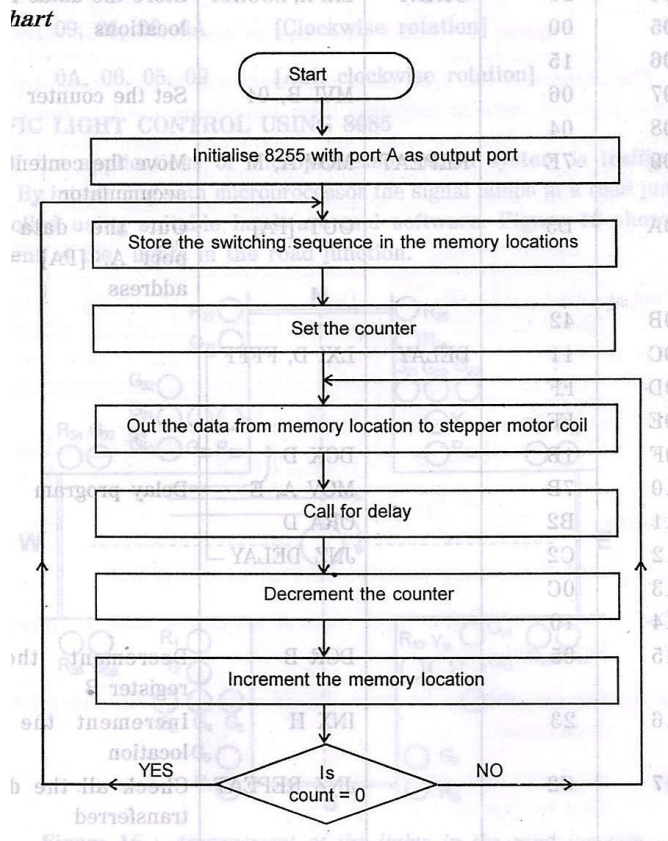
Table 5 : Half-stepping scheme

Step	A ₁	A ₂	B ₁	B ₂	
1	1	0	0	0	(08)
2	1	0	1	0	(0A)
3	0	0	1	0	(02)
4	0	1	1	0	(06)
5	0	1	0	0	(04)
6	0	1	0	1	(05)
7	0	0	0	1	(01)
8	1	0	0	1	(09)

Algorithm:

- Step1: initialize PPI 8255 with Port A as Output port
- Step2: store the switching sequence in the memory.
- Step3: set the counter to store the number of data.
- Step4: Send the first data to the stepper motor through Port A
- Step5: call subroutine for delay
- Step6: repeat steps 4 & 5 till the counter is zero
- Step7: repeat step 2 to 6 for continuous rotation of stepper motor.

FLOW CHART:



Program:

```

    MVI A, 80
    OUT [CR]
START LXI H, LOOKUP
    MVI B, 04
REPEAT MOV A, M
    OUT [PA]
DELAY LXI D, FFFF
    DCX D
    MOV A, E
    ORA D
    JNZ DELAY
    DCR B
    INX H
    JNZ REPEAT
    JMP START
LOOKUP
  
```

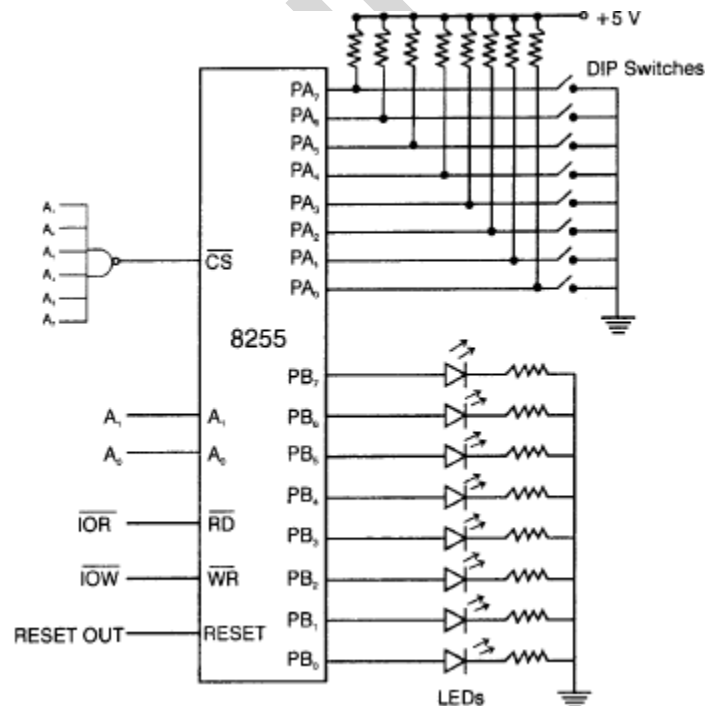
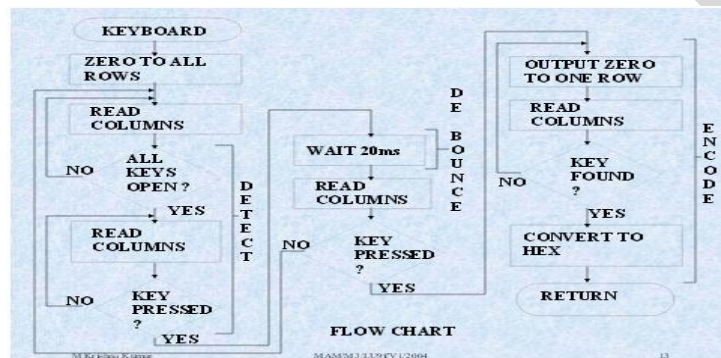
1500	09	05	06	0A	[CLOCKWISE ROTATION]
1500	0A	06	05	09	[ANTI CLOCKWISE ROTATION]

4. Write short notes on keyboard interfacing. (AUC NOV 2011)

Keyboard Interfacing:

A pushbutton keyboard is connected to port A & a seven segment LED is connected to port B of the 8255A. port A should be configured as an input port and port B as an output port. This is a simple I/O configuration in mode0 without the use of handshake signal.

The 8085 microprocessors interfaced with input devices (DIP switches) and output devices (LED, LCD) using 8255 PPI. Fig.4.15 shows the interfacing of DIP switches and LEDs with microprocessor.



Port A is configured as input port and Port B is configured as output port. When no DIP switch is pressed, all the bits in Port A will be high, because these are connected to +5V through pull up resistors. If any DIP switch is pressed, current will flow through that switch through the corresponding resistor and the voltage will drop to 0V. So the corresponding bit in the port will be zero. By reading the Port A at regular interval, we can identify the switches pressed.

The Port B lines are connected to LEDs through protecting resistors. The other end is connected to ground. When logic 1 is sent to any port B line, the LED will conduct current and it will glow. When logic 0 is sent to Port B then the LEDs will be off.

The \overline{IOR} signal connected to the \overline{RD} pin of 8255 makes the input port can have only IO addressing i.e. it can use only IN port instruction. Similarly \overline{IOW} signal connected to \overline{WR} pin of 8255 makes the output port (Port B) respond only to the OUT port instruction.